Welcome To

ISSCC 2014
Session 12
Sensors, MEMS and Displays

3D Ultrasonic Gesture Recognition

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[3]Chirp Microsystems, Inc., Berkeley, CA

Contextual Awareness

What is going on in the space around me?

Mobile Gesture Recognition

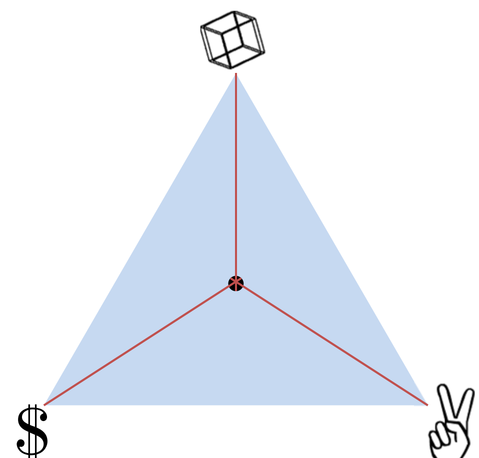
chillingo.com

Potential New Applications

- Mobile Games (e.g. 3D Catapult – see demo)
- Situations where touch isn't appropriate
  - e.g. car dashboard, greasy fingers
- UI for tiny mobile devices (Google Glass, Smart Watch)

Wish list

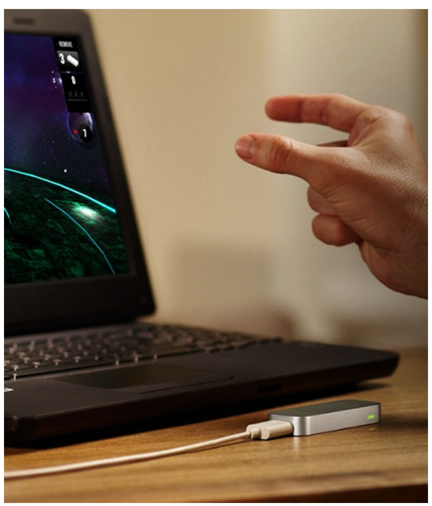
- Small (low power)
- Optimal Resolution / Working Range
- Solution cost $



Gesture Recognition

First

Microsoft Kinect



LEAP motion // leapmotion.com

Now

Samsung S4 // samsung.com

Google Glass//google.com

iRing// yankodesign.com

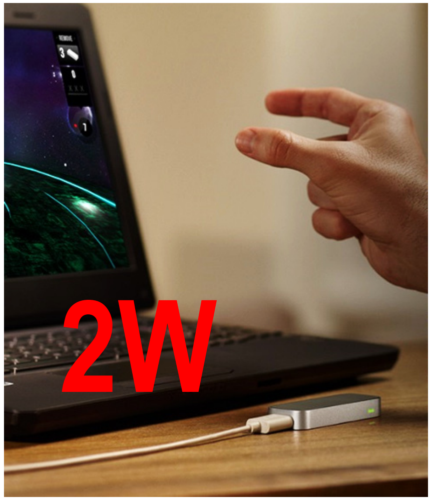
Soon?

Galaxy Gear // samsung.com

Gesture Recognition

First

Microsoft Kinect



LEAP motion // leapmotion.com

Samsung S4 // samsung.com

Size $\frac{1}{100}$

Power $\frac{1}{10000}$

Cost $\frac{1}{100}$

Google Glass//google.com

iRing// yankodesign.com

Soon?

Galaxy Gear // samsung.com

Contextual Awareness – How do we do it?

Size $\frac{1}{100}$ **Power** $\frac{1}{10000}$ **Cost** $\frac{1}{100}$

Situational Awareness

Light

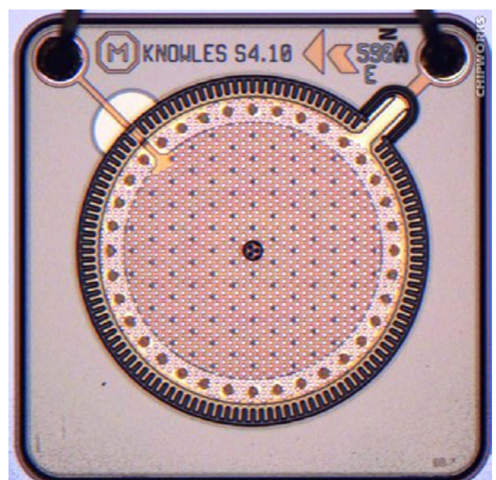
- 👍 100mm^3
- 👍 Ambient light
- 👎 >>200mW

Situational Awareness

Light

- $100mm^3$
- Ambient light
- >>200mW

Sound



- $9mm^3$
- 400µW
- Passive
  - not enough ambient sound

Emits ultrasound from mouth, receives in ears

Specialized brain circuits process echoes

Identifies insects from wing velocity

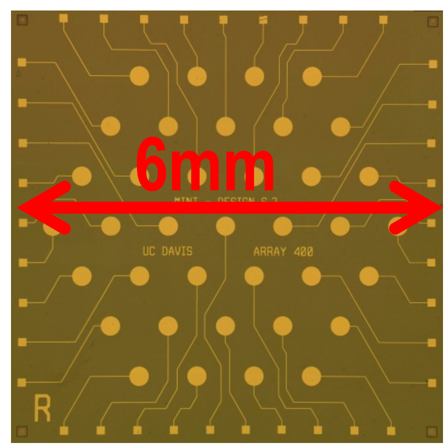
Targets mosquitoes from 800mm away

[D.R. Griffin, J. Animal Behaviour, 1960]

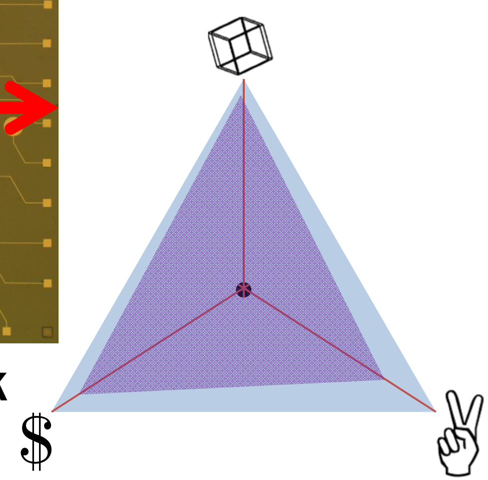
Ultrasonic Gesture Recognition

- Very low power (μW … mW)
  - always on (serve as “on” switch)
- Small (~ microphone)
  - fits devices that are too small to accommodate a display
- Good depth resolution
- Limited (~2m) range
  - best for close interaction
- Limited angular resolution

maxbotix.com



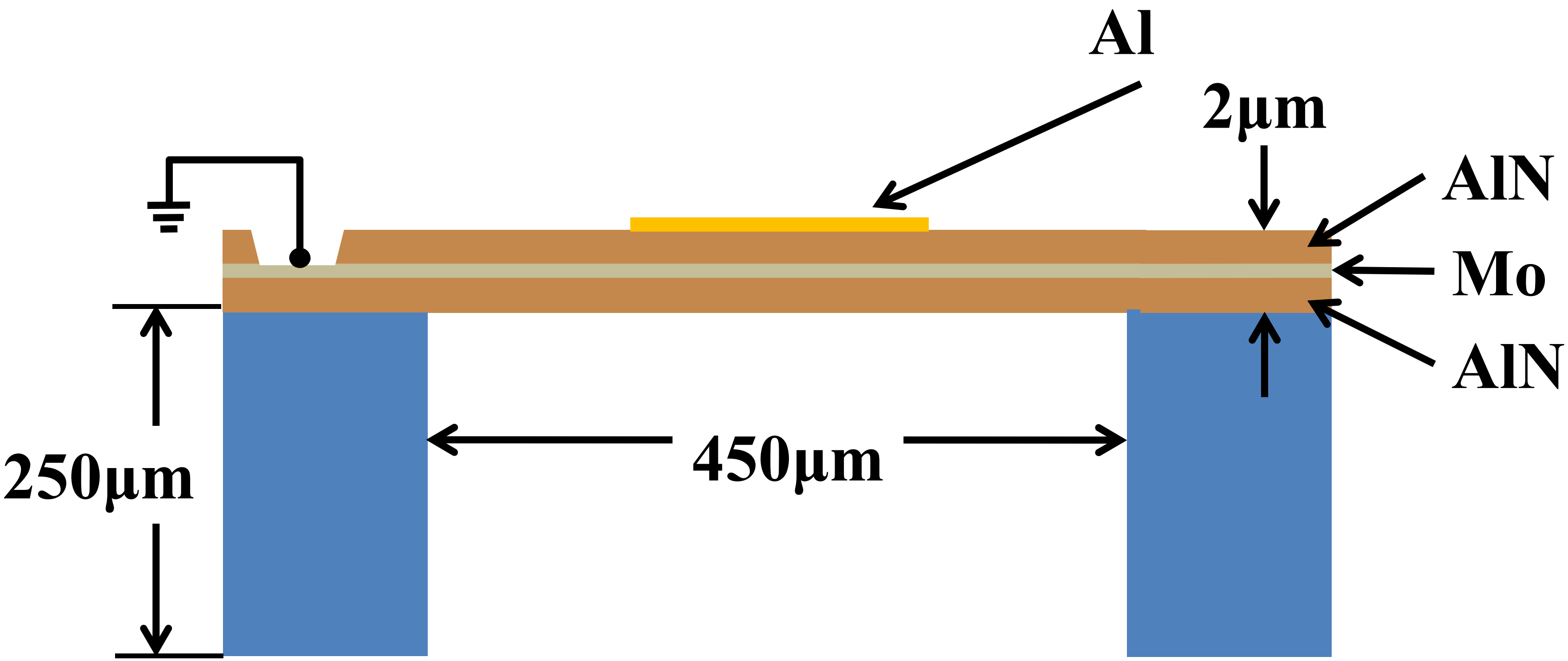
Chirp: our work



Outline

1. Transducer Operation
2. Depth Sensing
3. Interface Circuits
4. Results

AlN pMUT Operation



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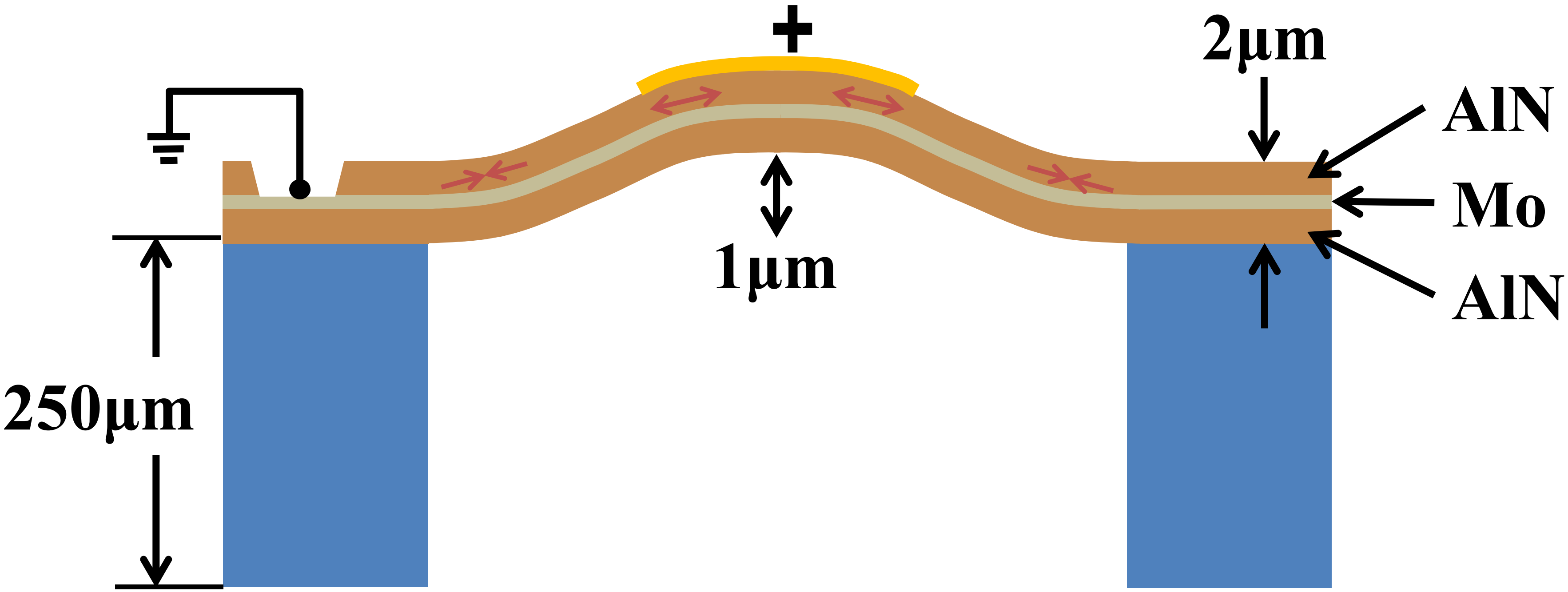

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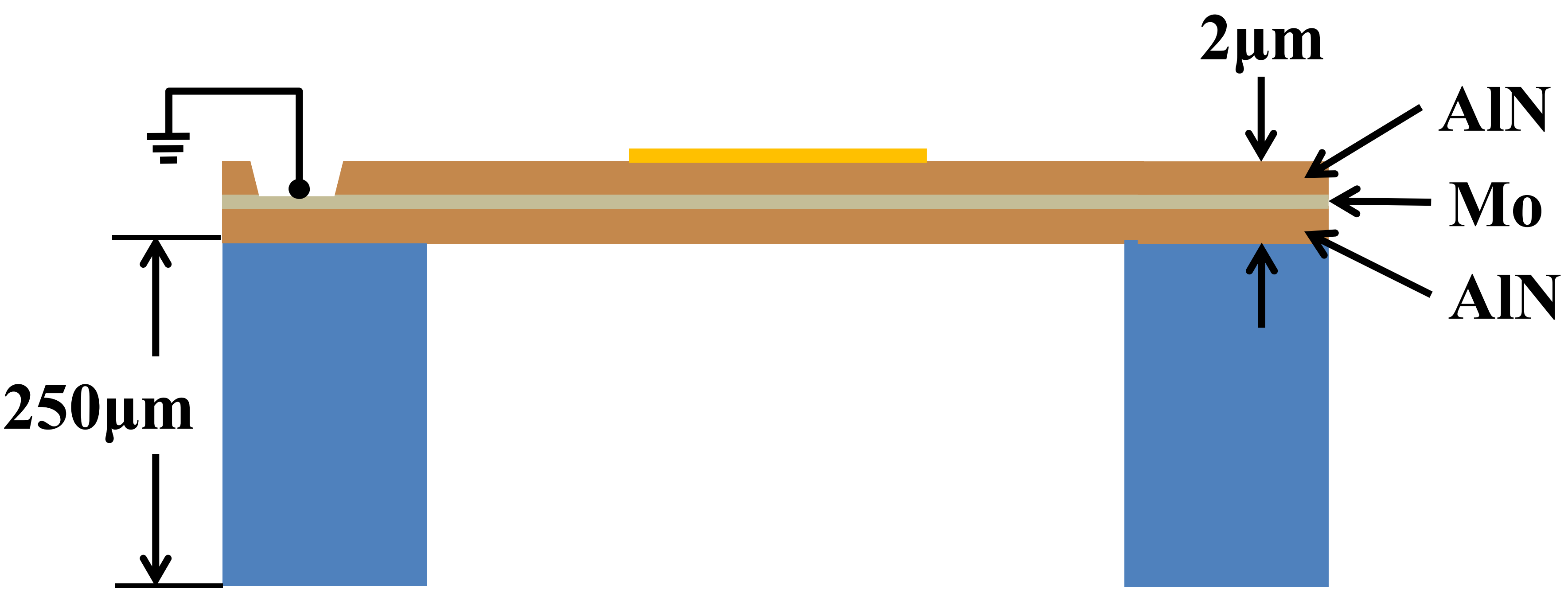

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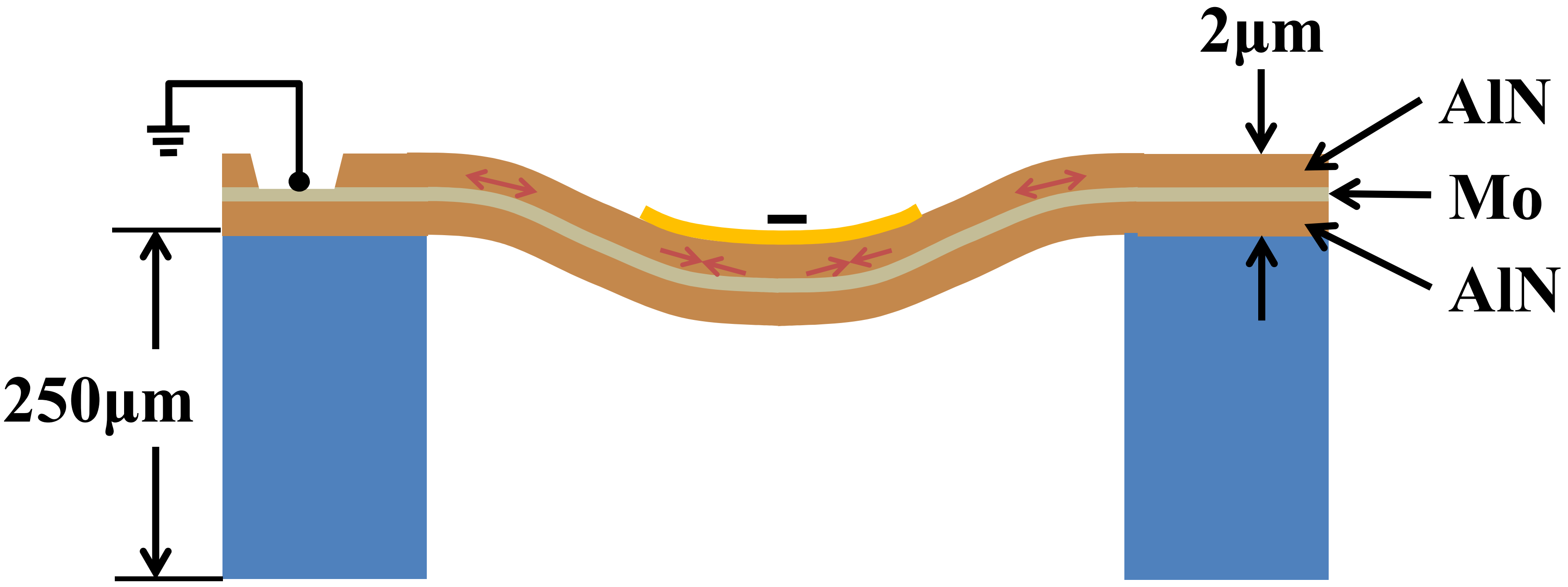

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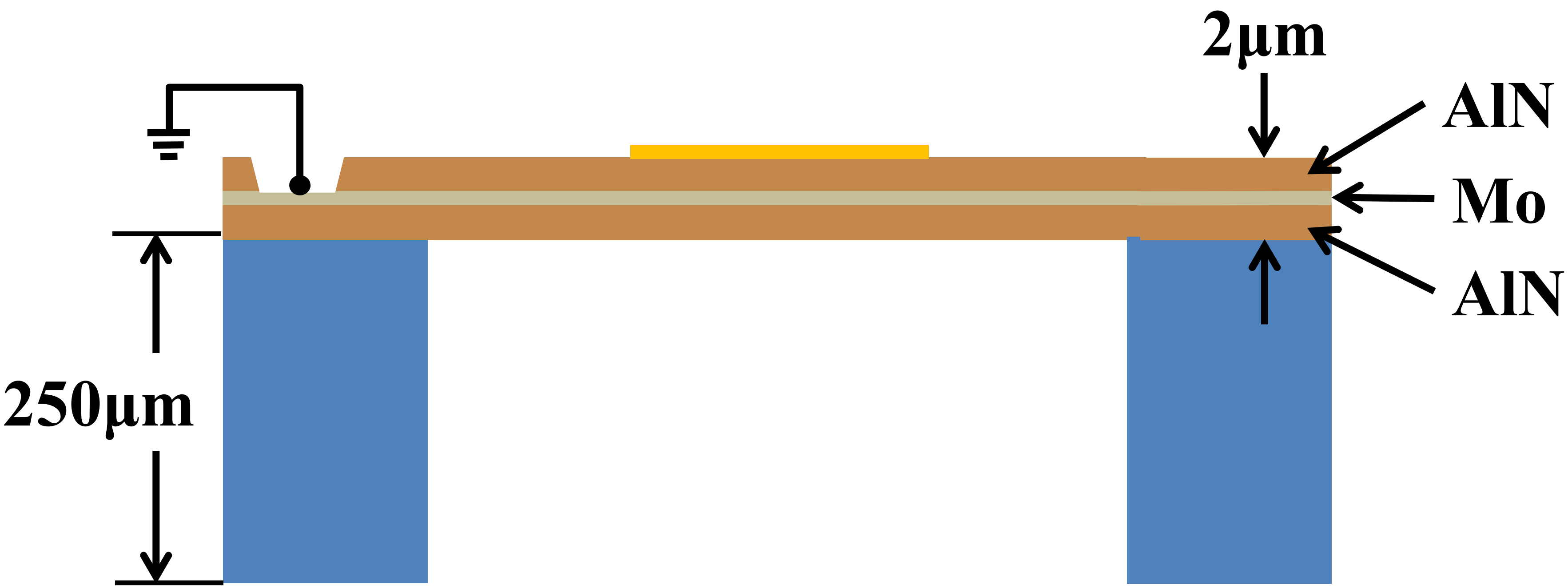
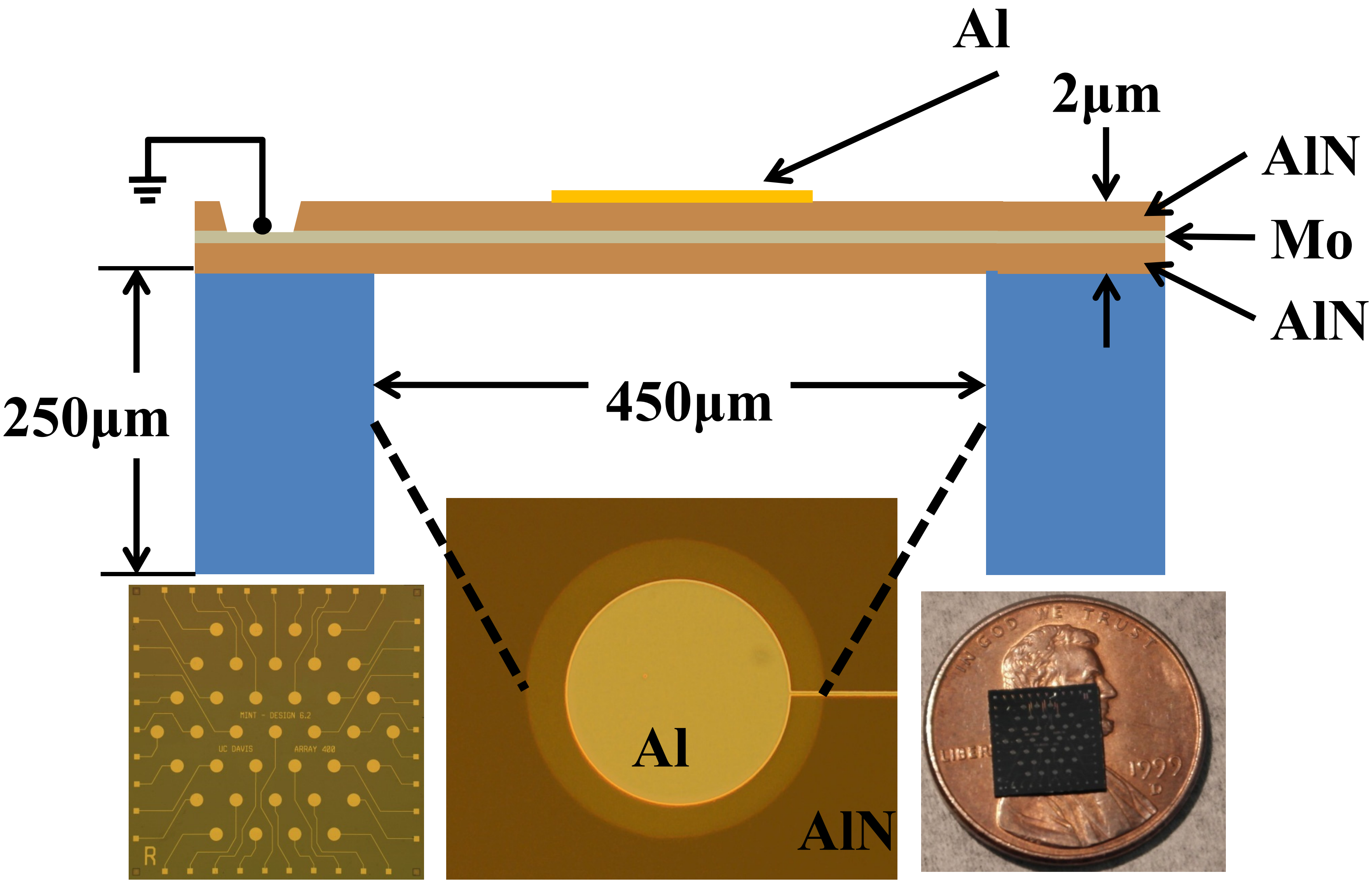


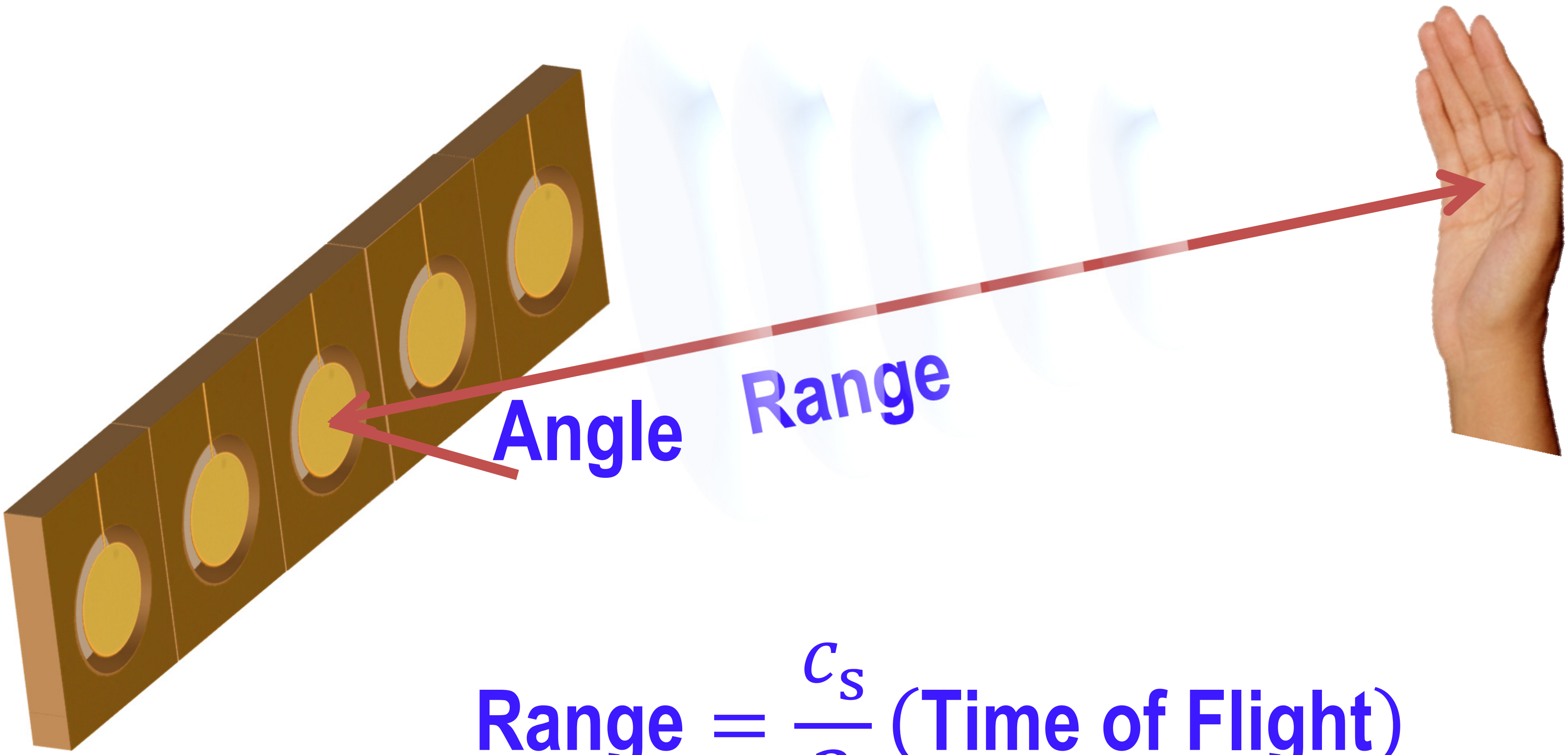
$f_o \approx$ 220kHz

BW ≈ 12kHz

AlN pMUT Operation



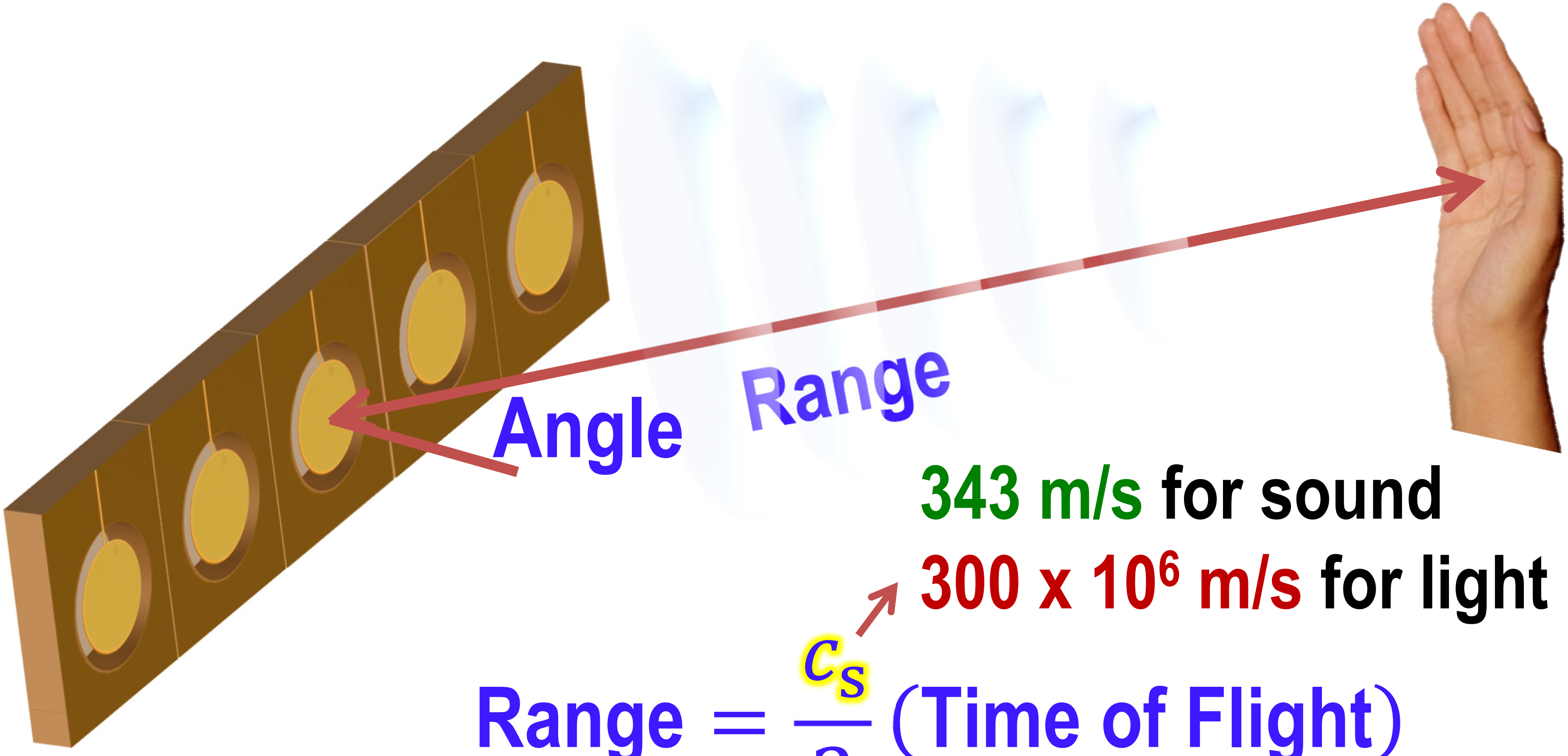
Depth Sensing



$$\text{Range} = \frac{c_s}{2}(\text{Time of Flight})$$

$$\text{Angle} \propto \Delta(\text{Time of Flight})$$

Depth Sensing



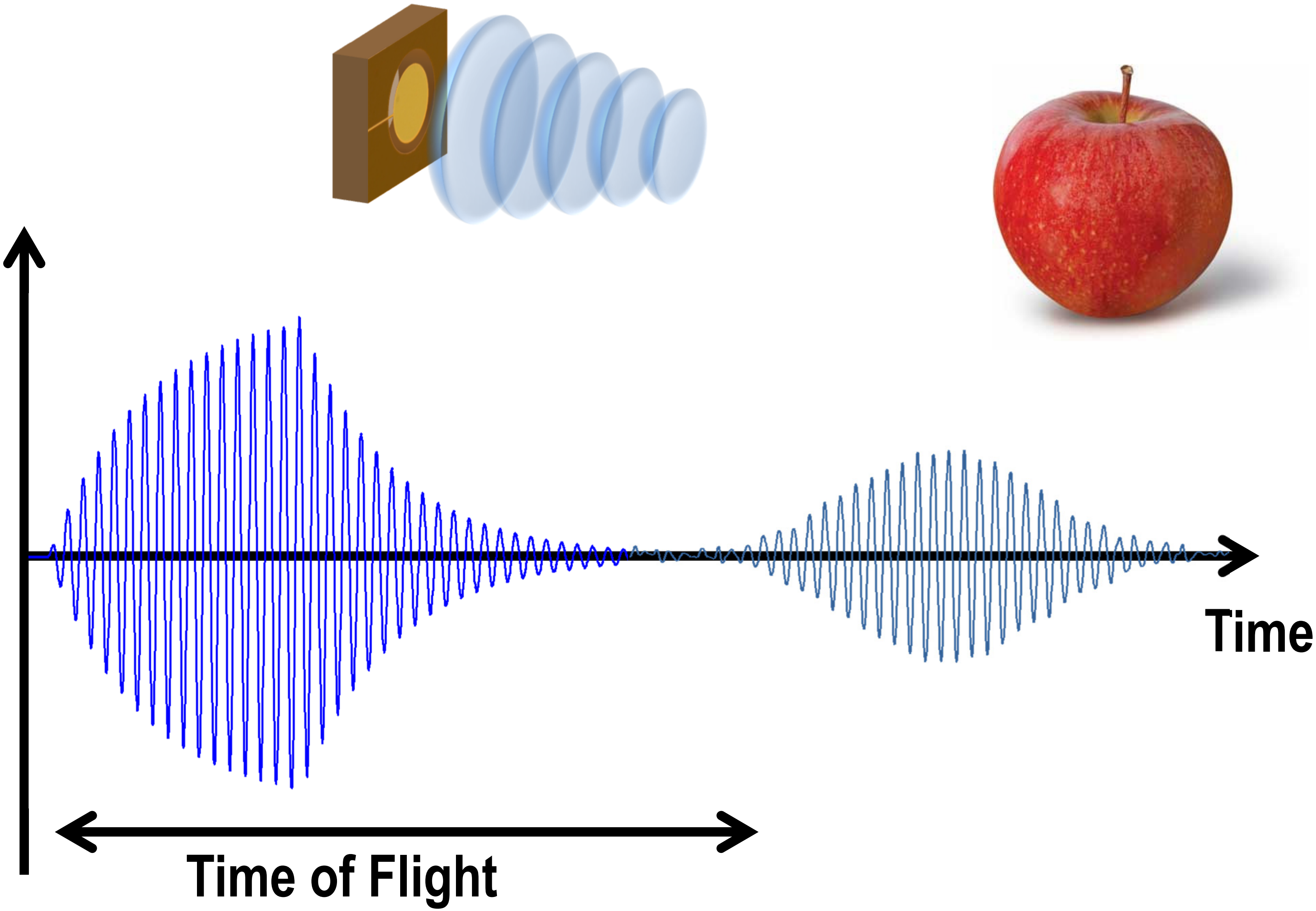
343 m/s for sound

300×10^6 m/s for light

$$\text{Range} = \frac{c_s}{2}(\text{Time of Flight})$$

$$\text{Angle} \propto \Delta(\text{Time of Flight})$$

Time of Flight Range Measurement



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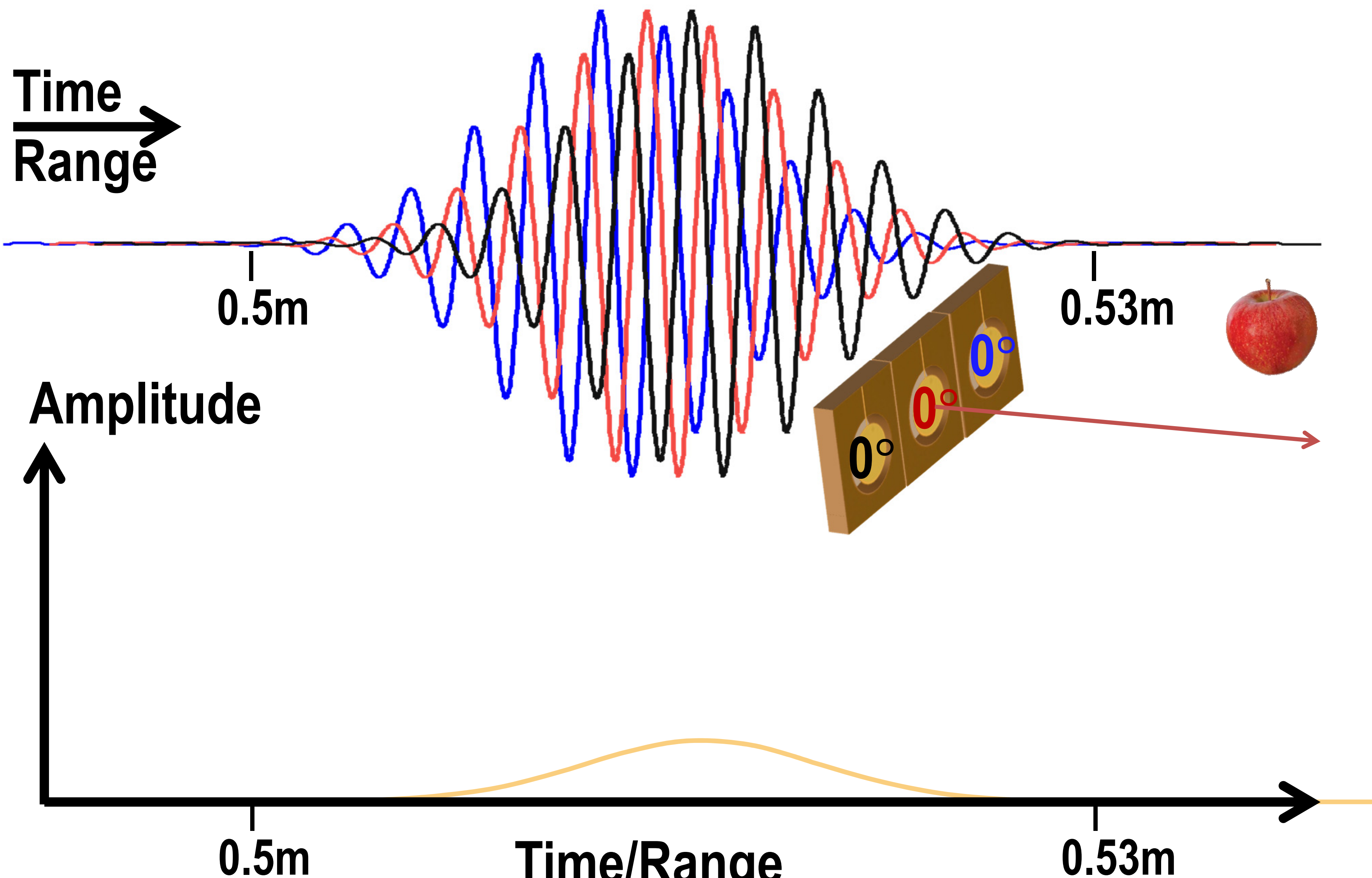
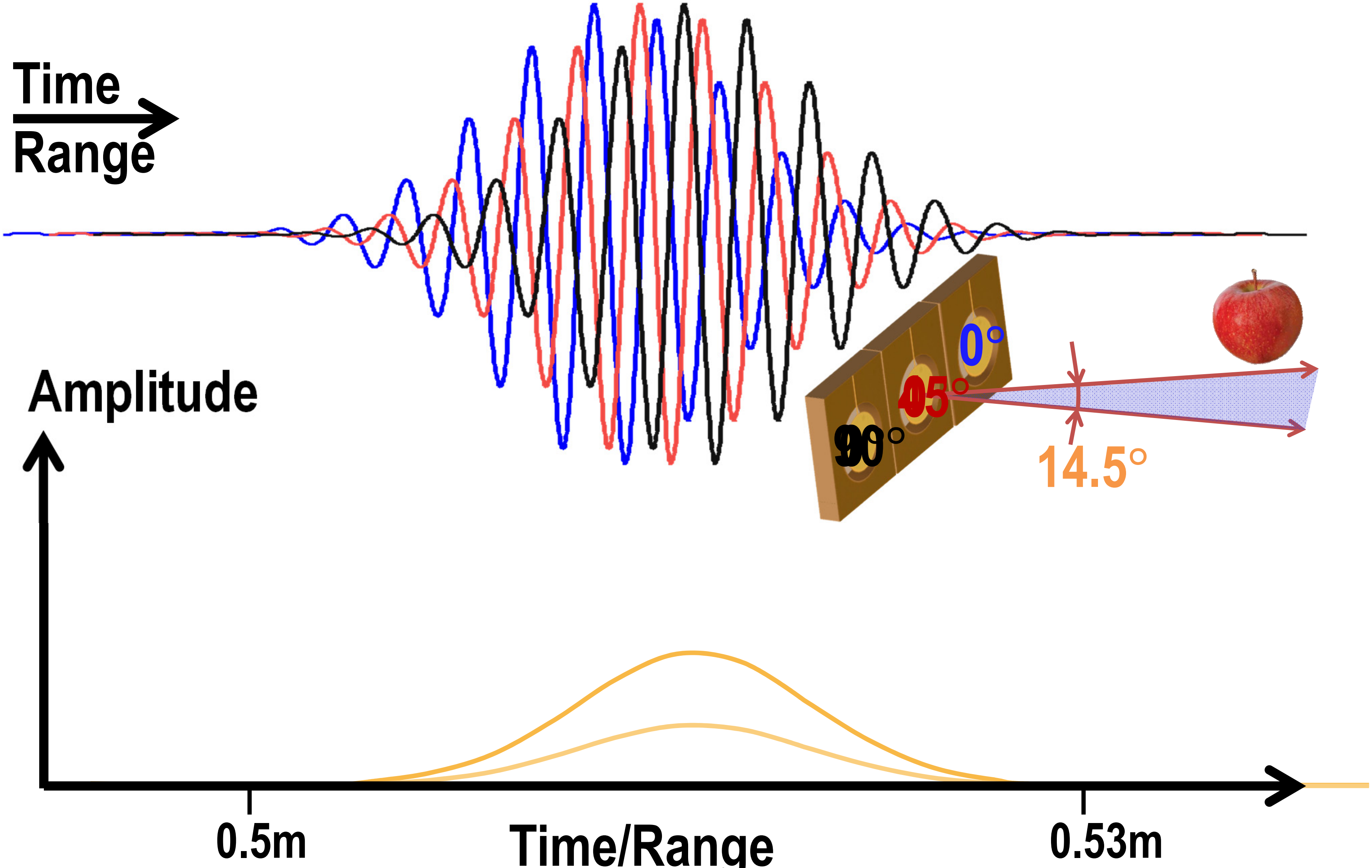
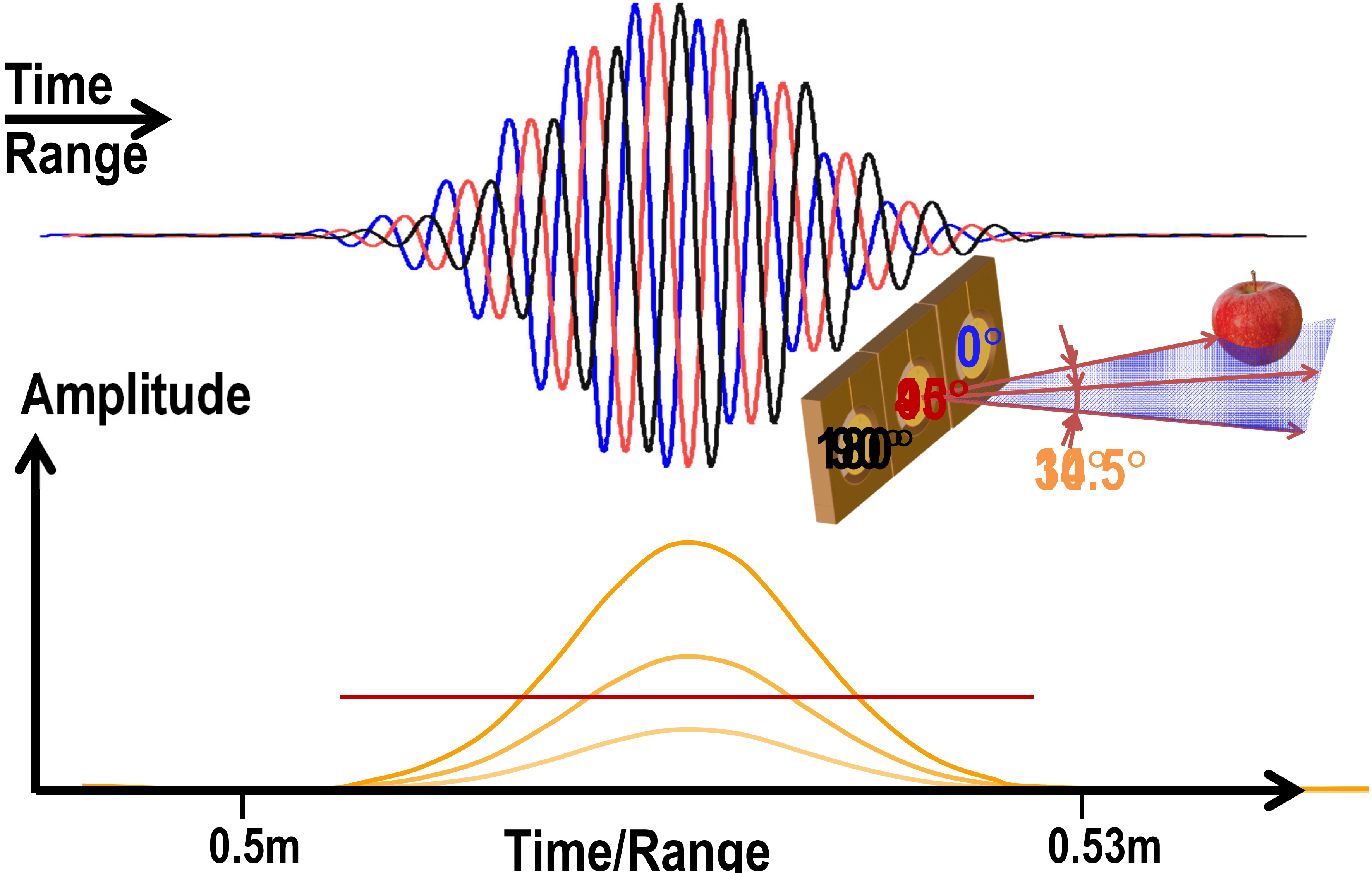
Receive Signal Beamforming



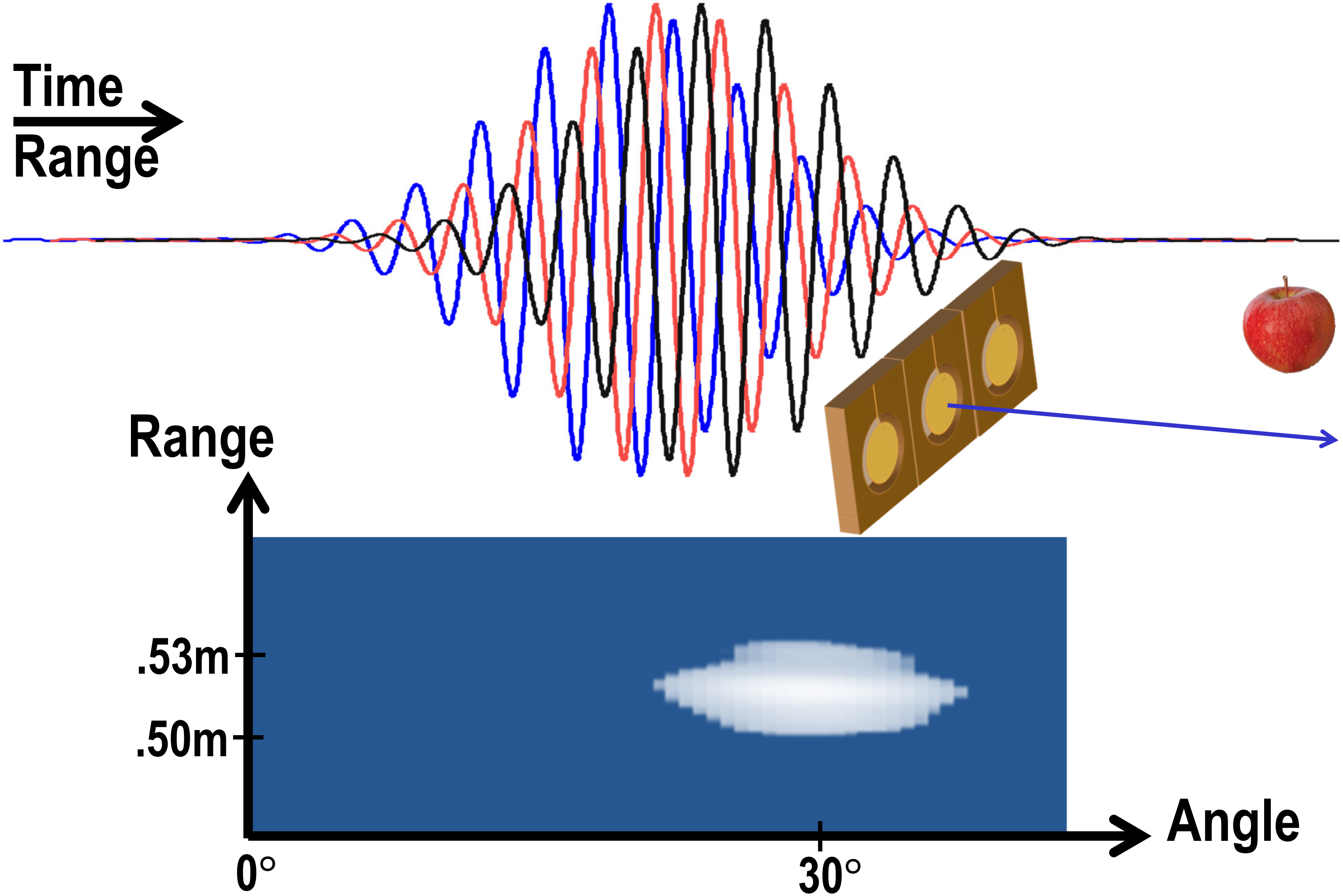
Receive Signal Beamforming



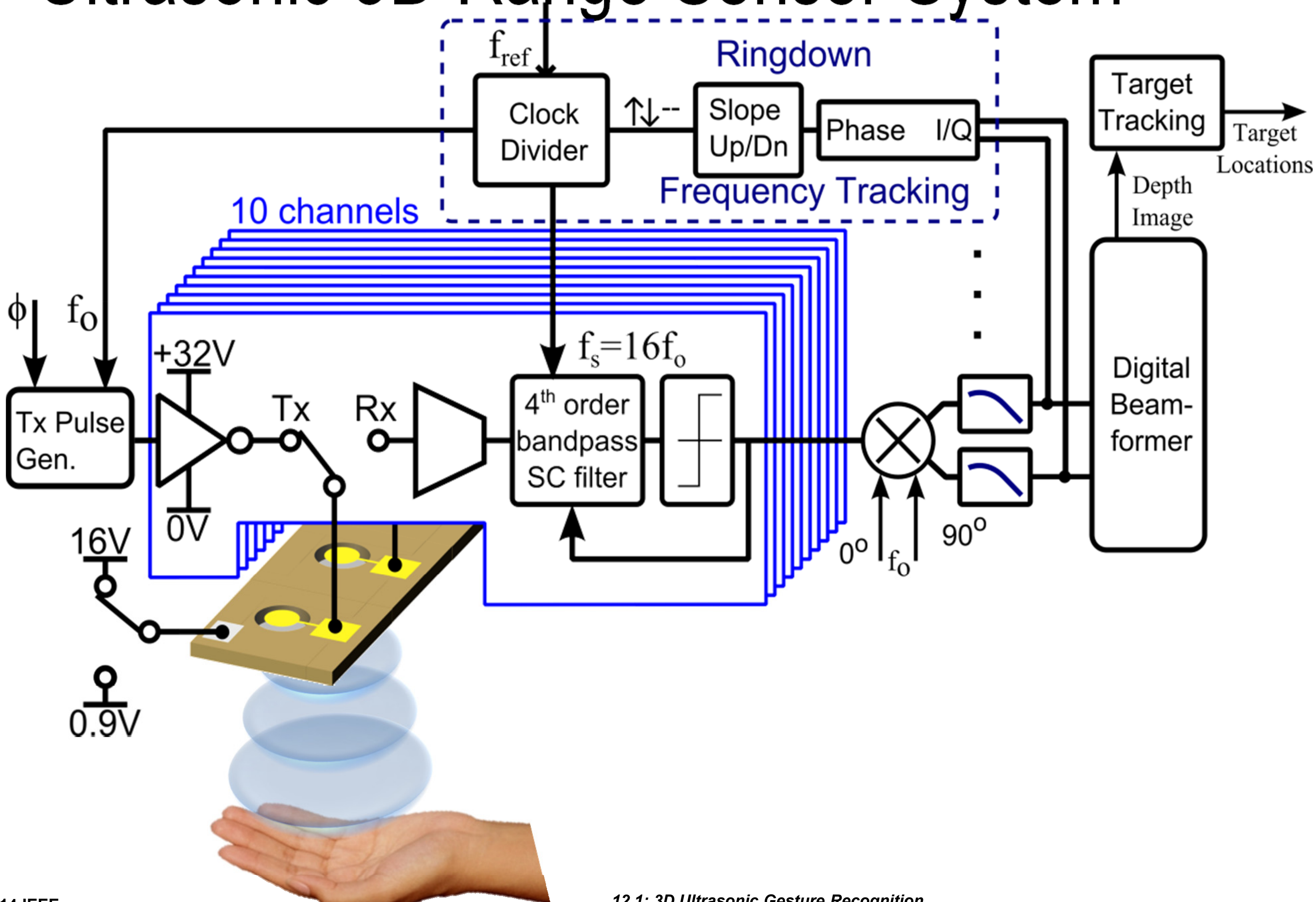
Receive Signal Beamforming



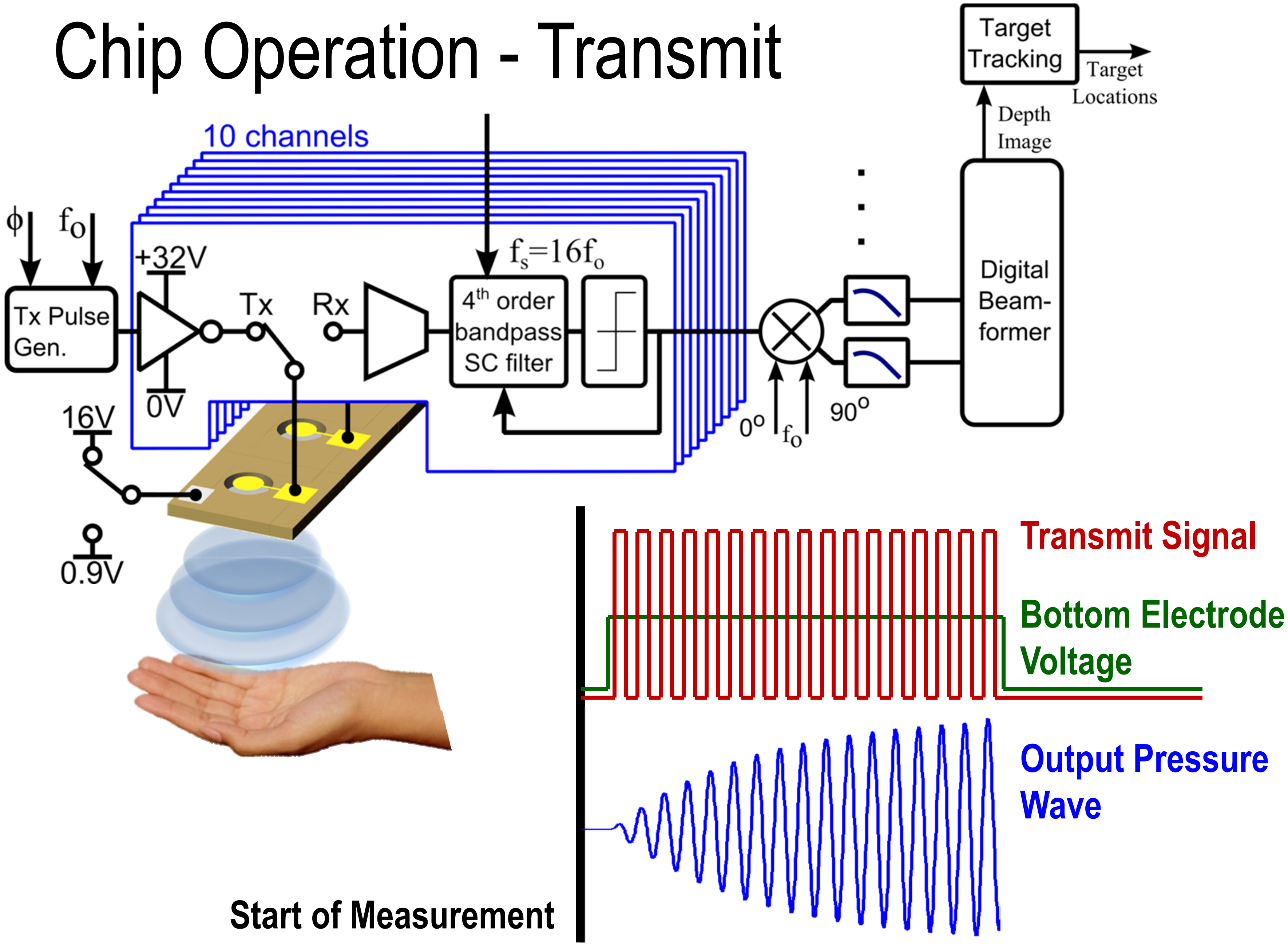
Receive Signal Beamforming



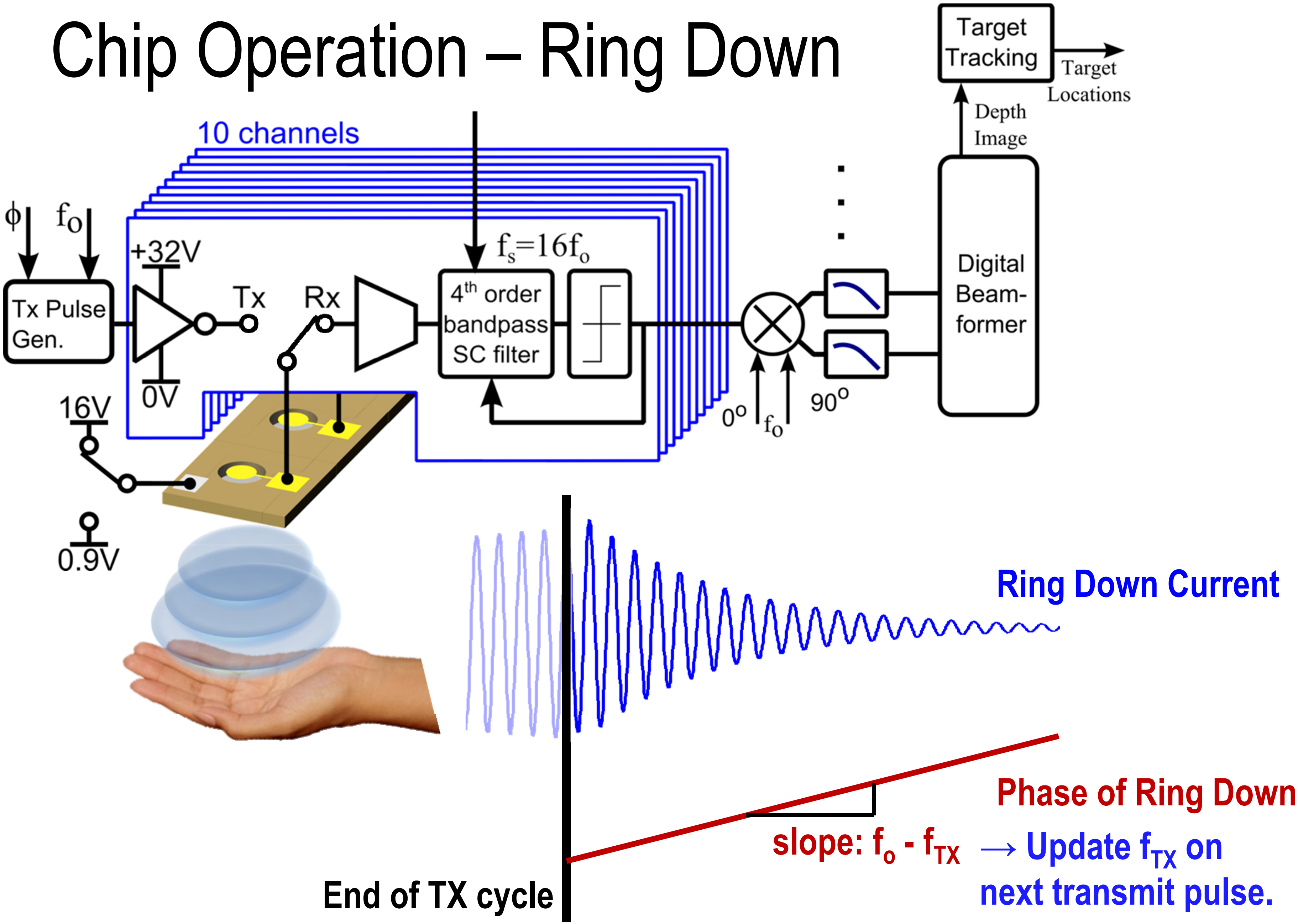
Ultrasonic 3D Range Sensor System



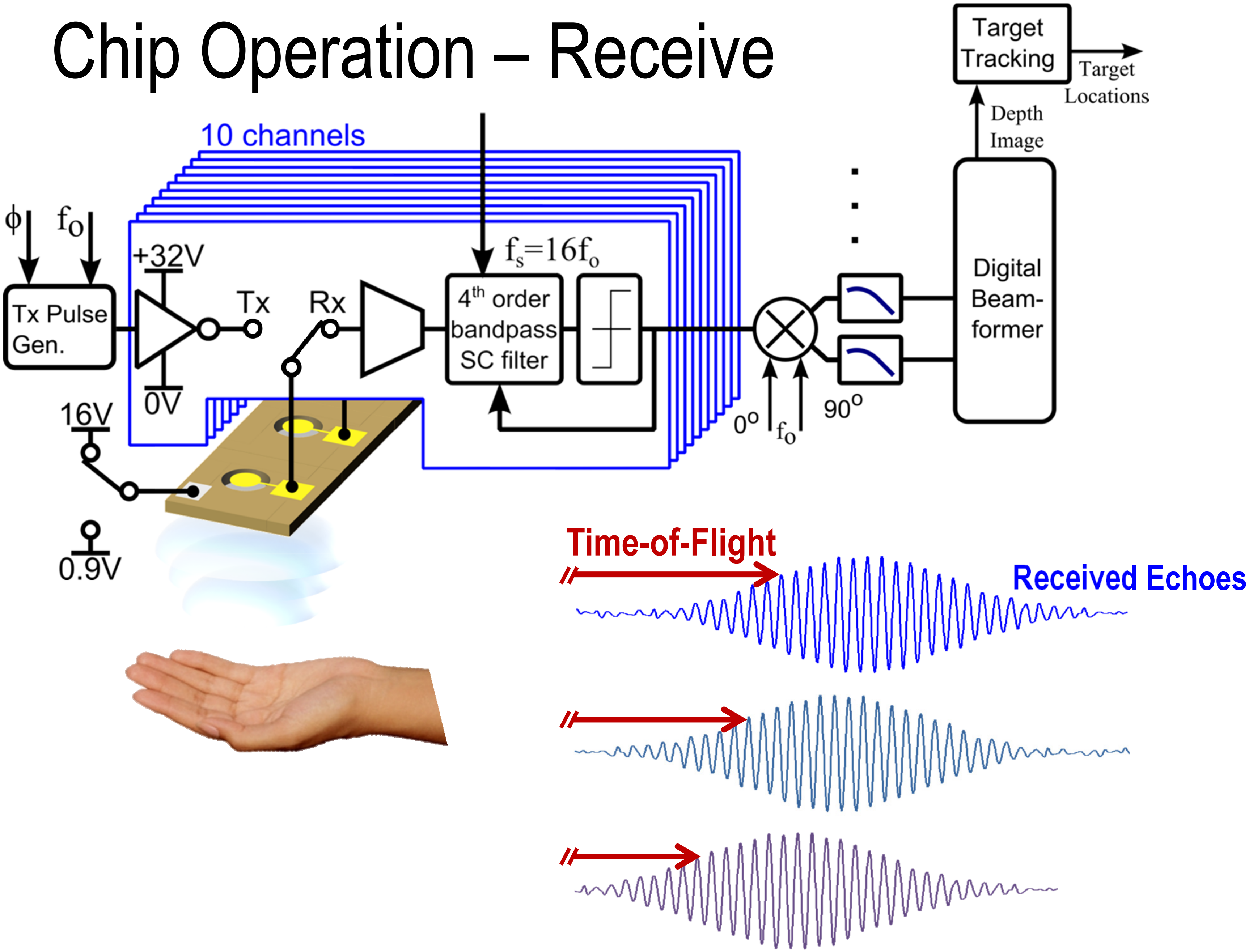
Chip Operation - Transmit



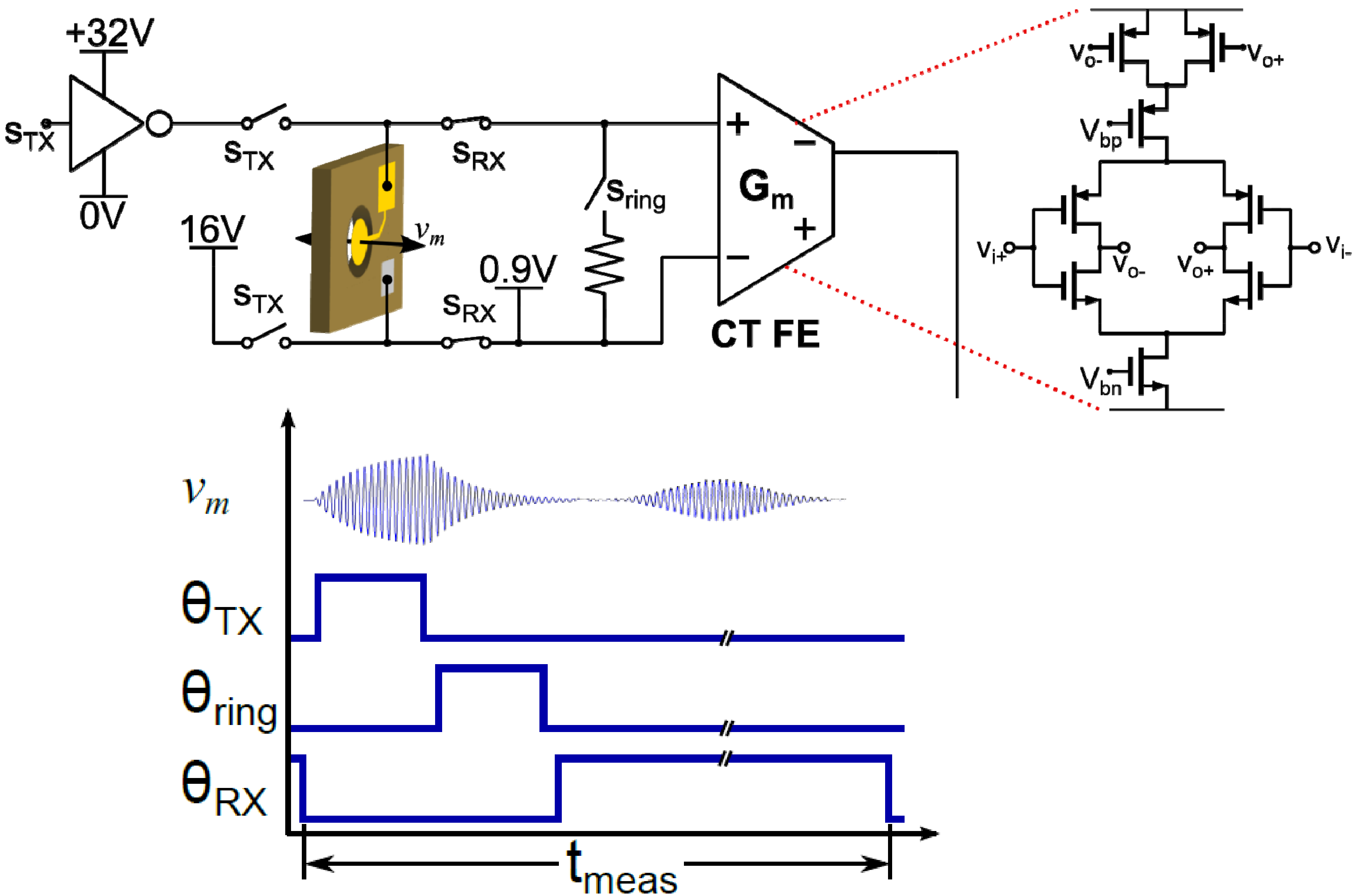
Chip Operation – Ring Down



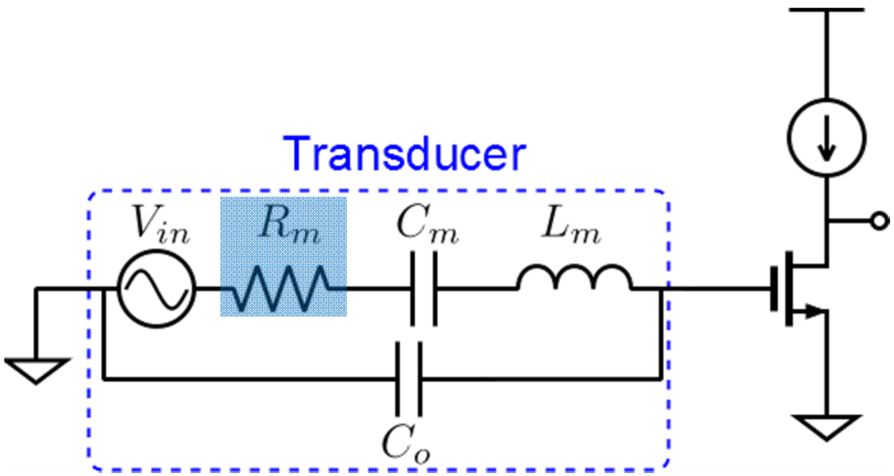
Chip Operation – Receive



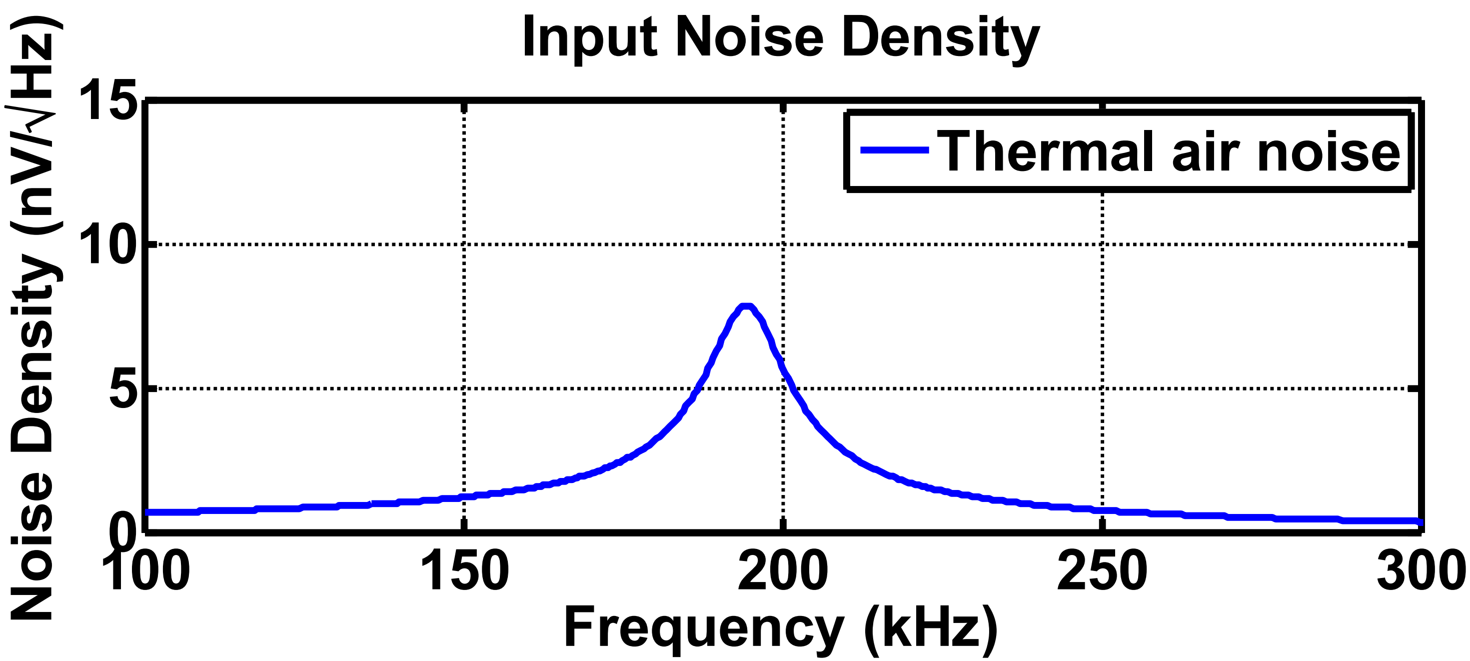
Front-end Circuit



Range Measurement – Noise



Receive Circuit



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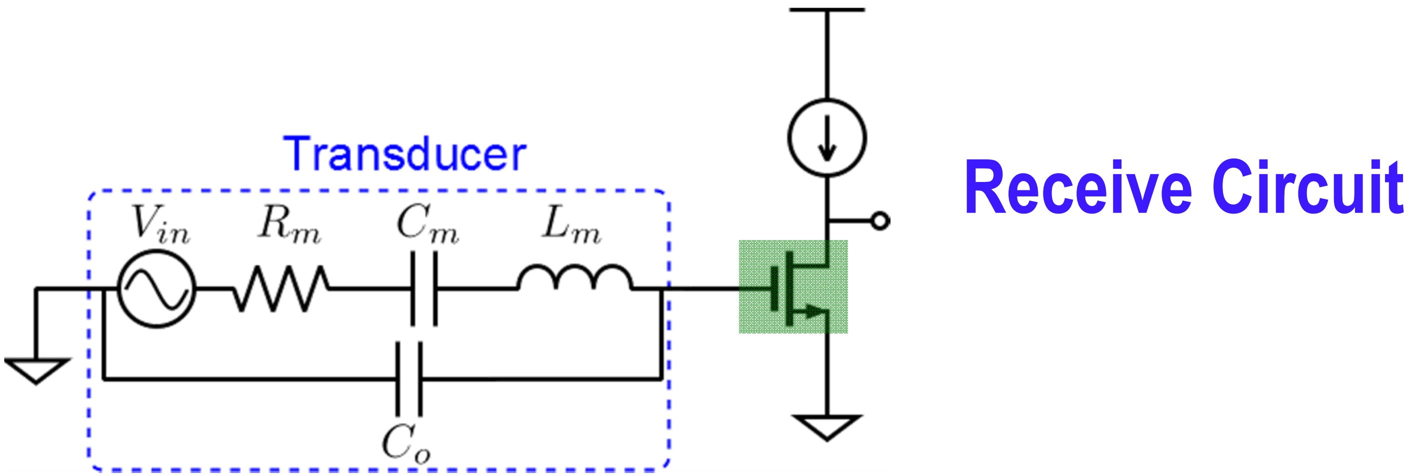
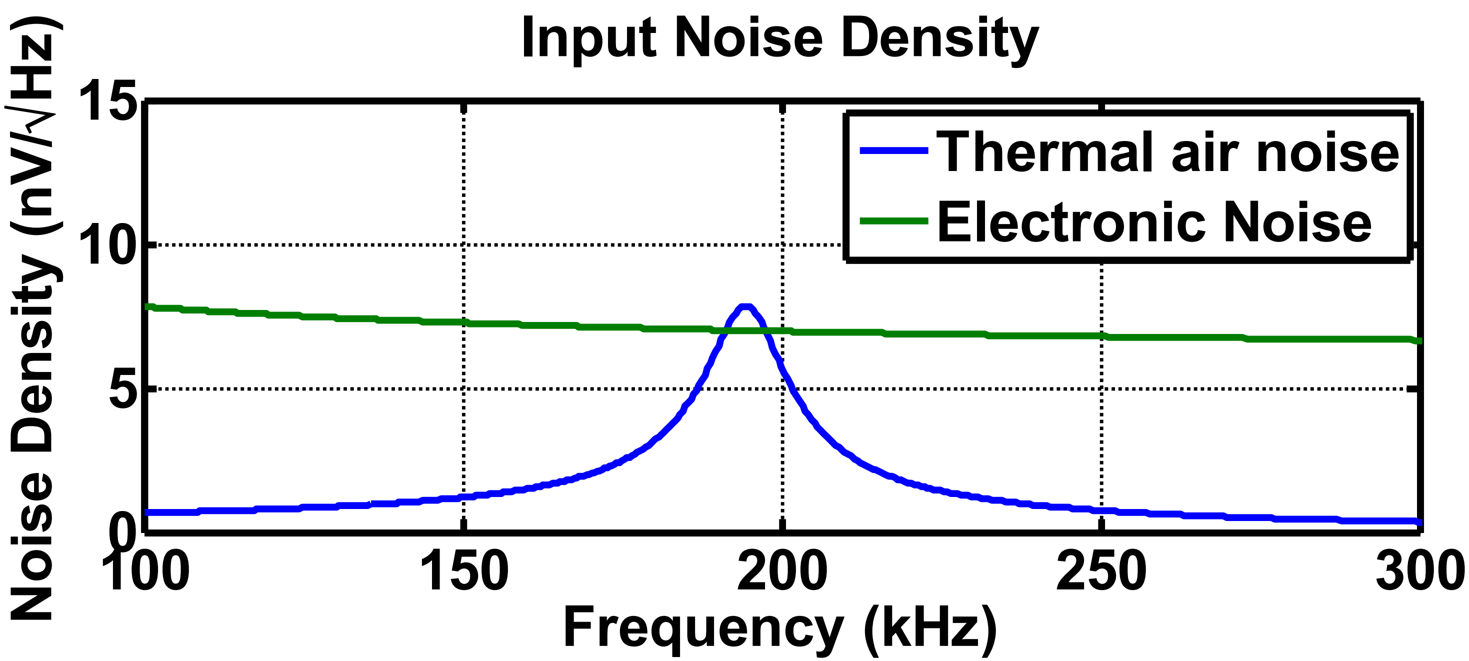
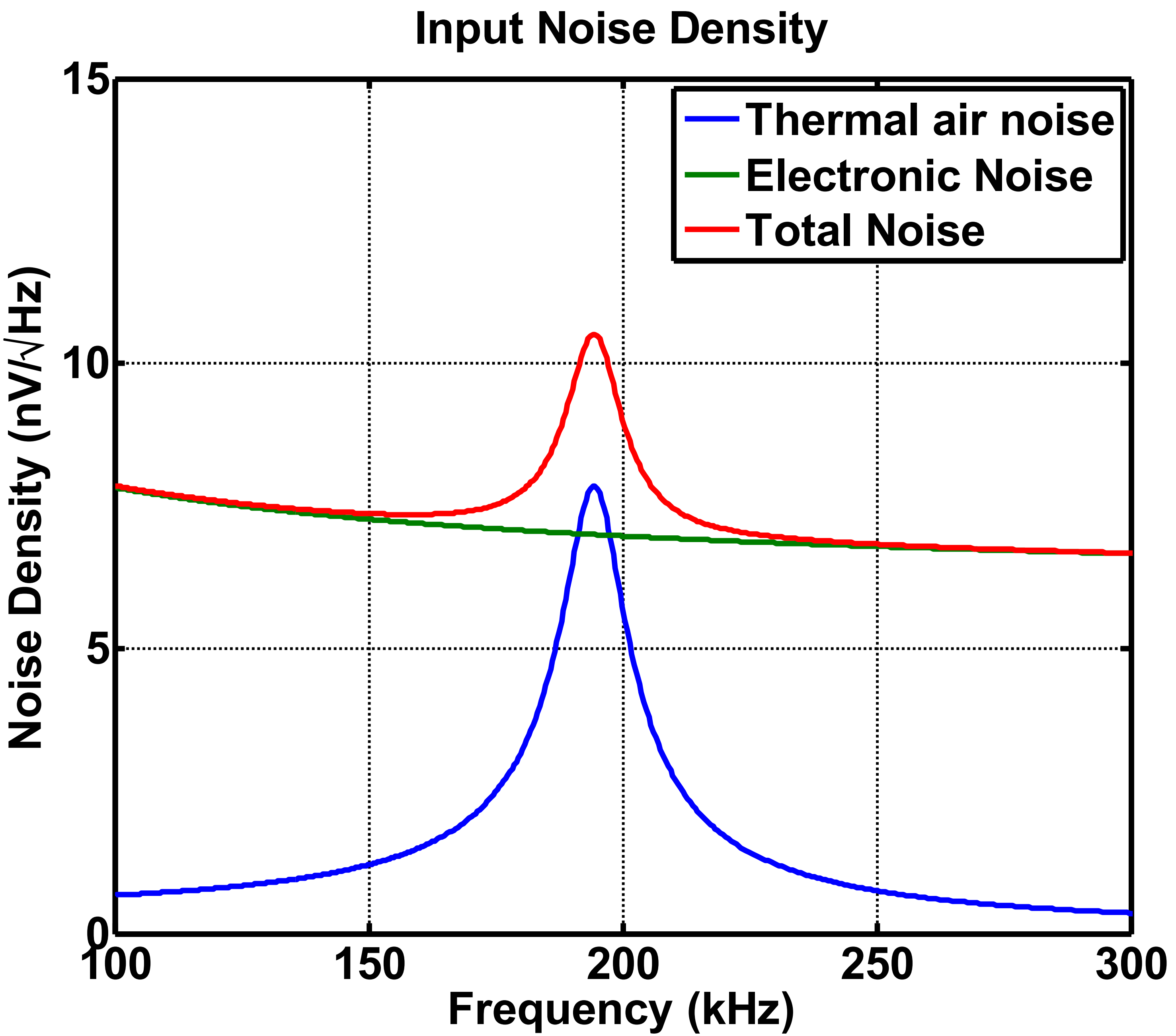
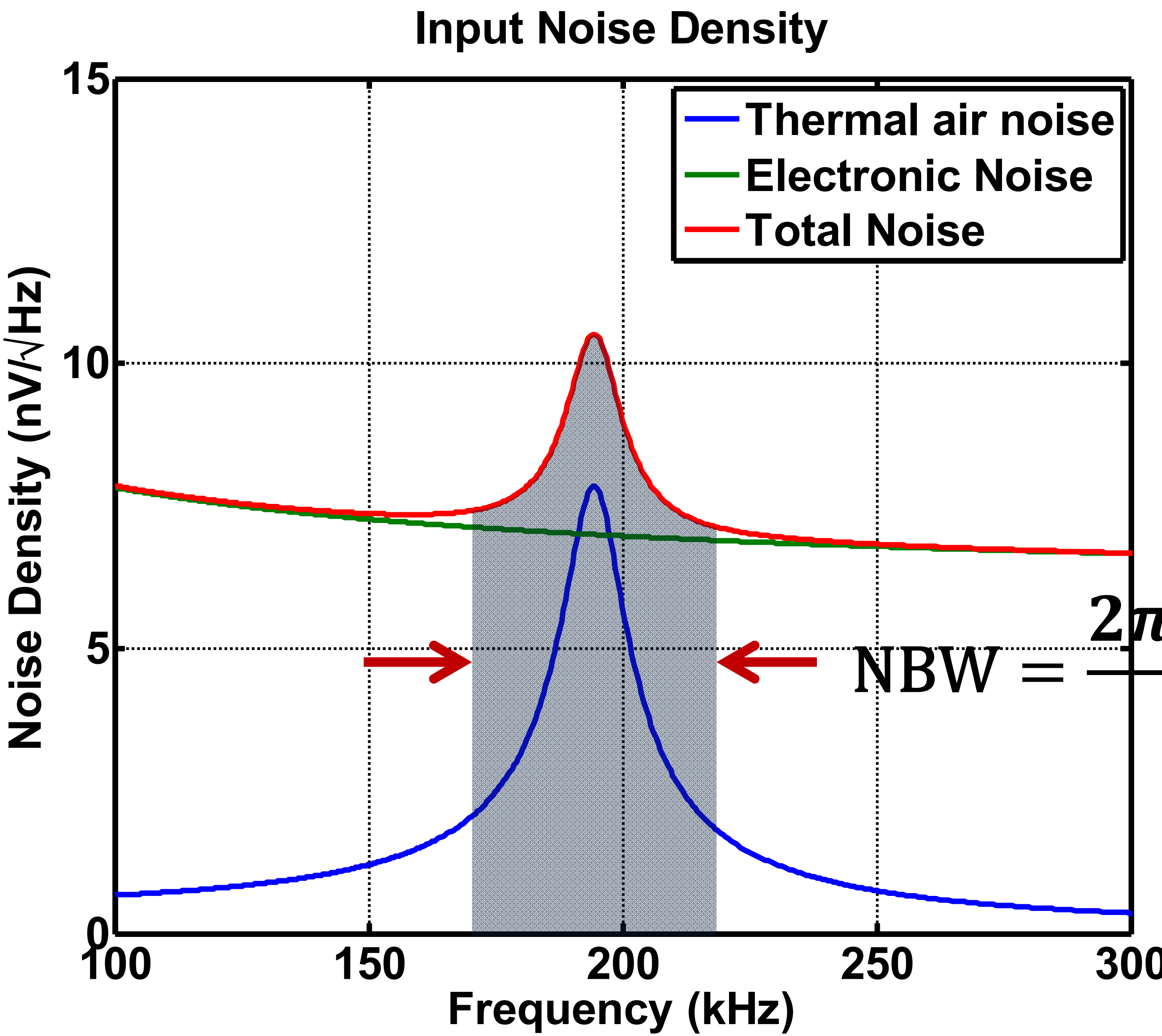


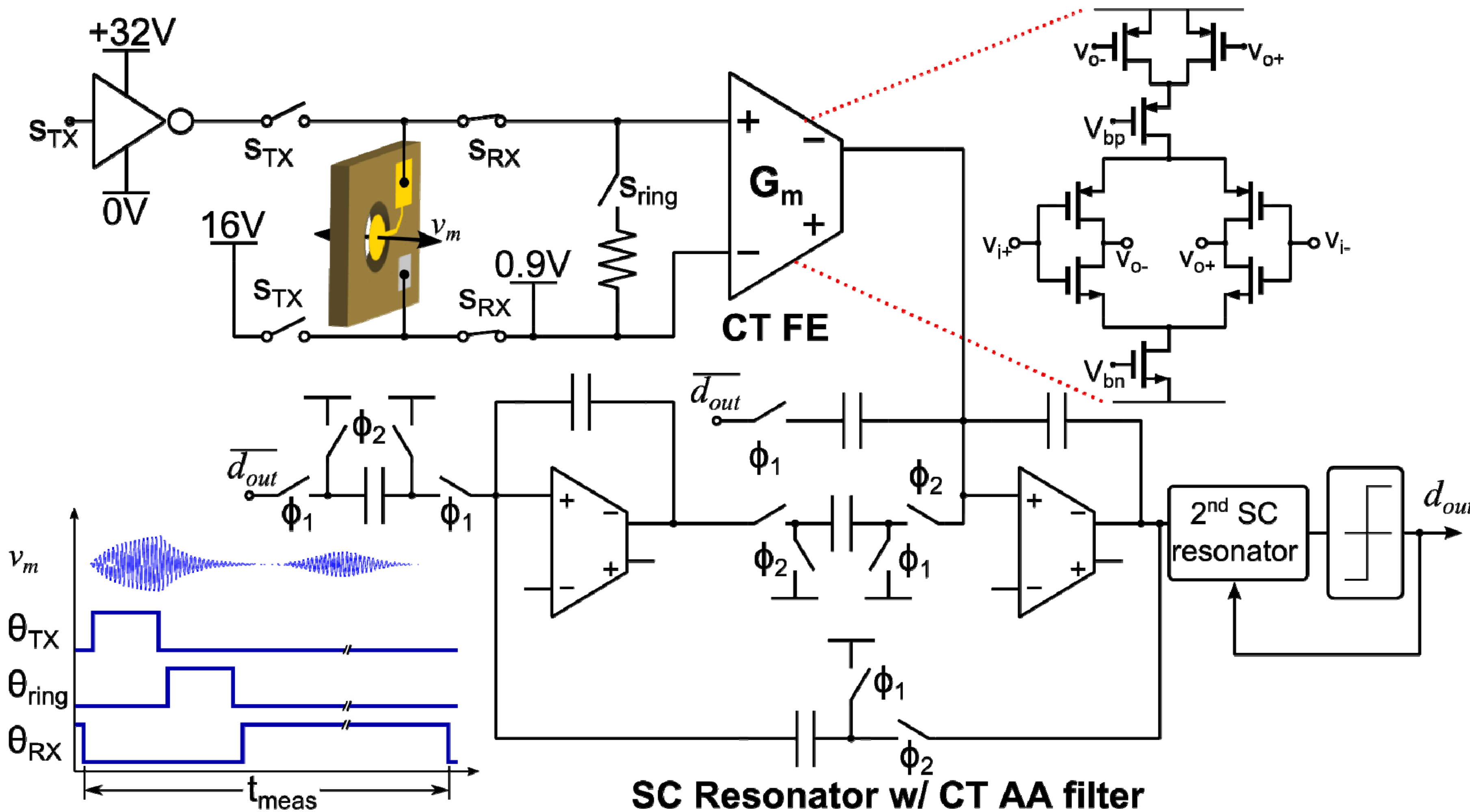



Input Noise Density
Thermal air noise
Electronic Noise
Total Noise
Noise Density (nV/√Hz)
15
10
5
0
100
150
200
250
300
Frequency (kHz)



$$\mathrm{NBW} = \frac{2\pi \mathrm{BW}}{4}$$

Single Channel Circuit



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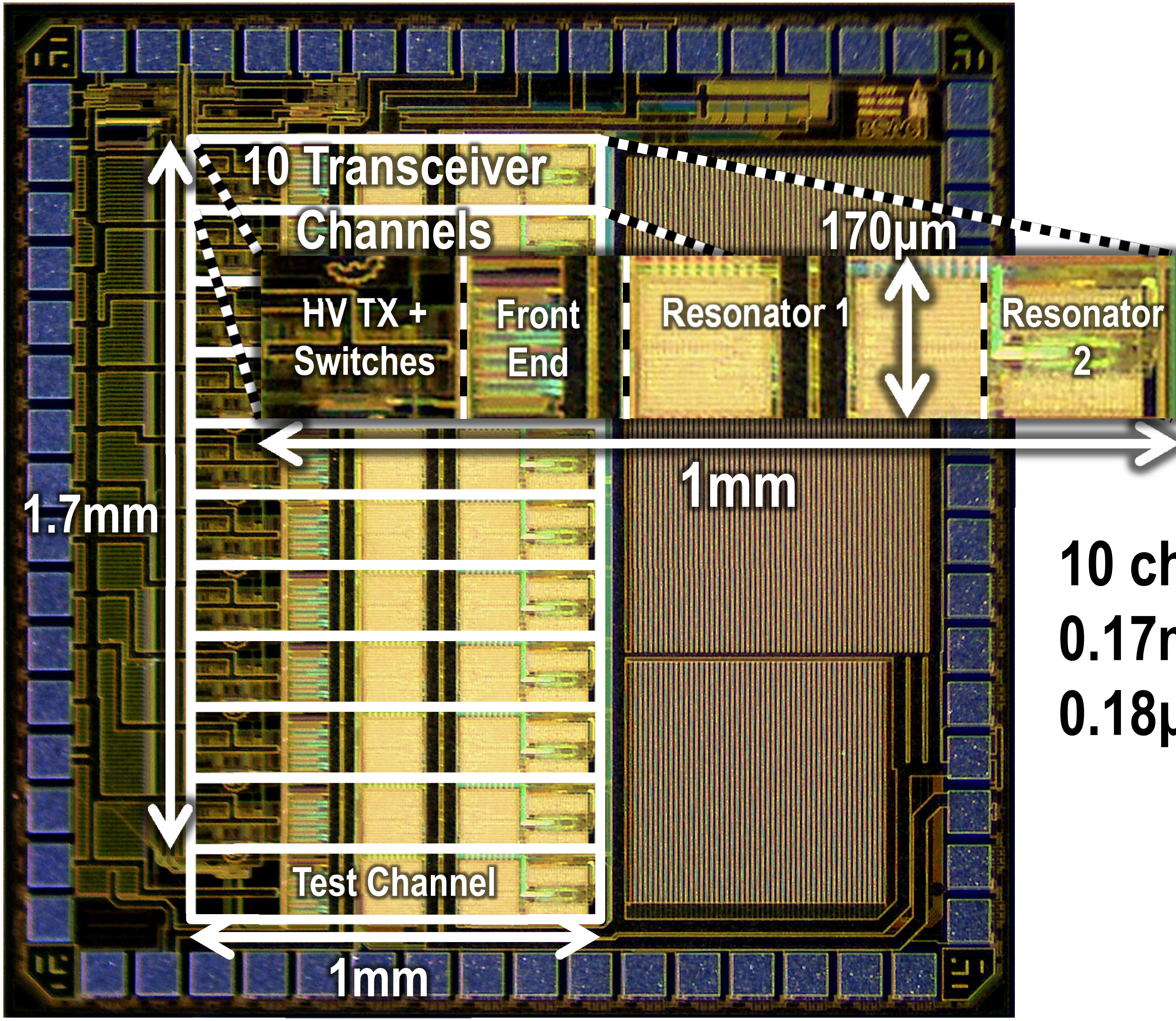
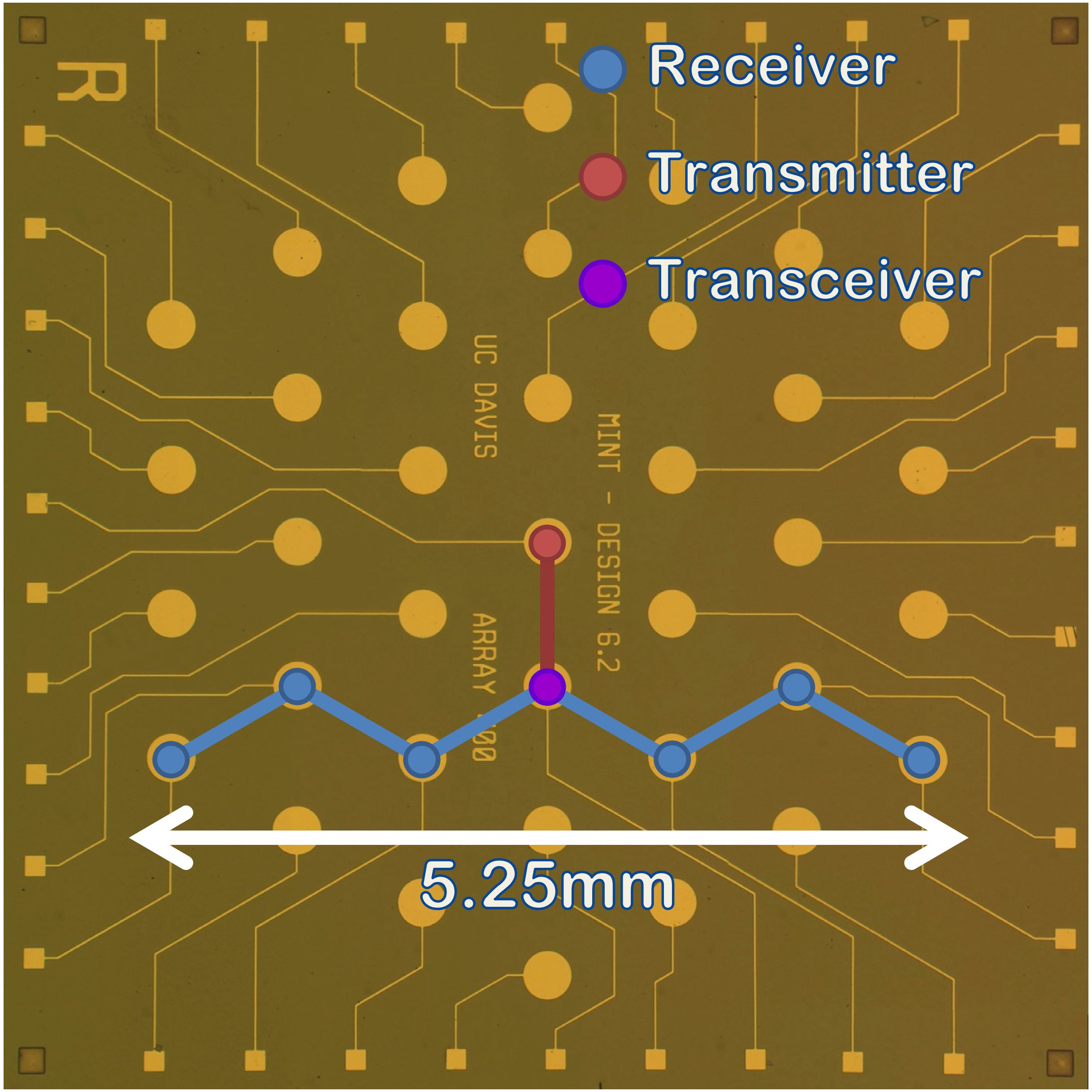
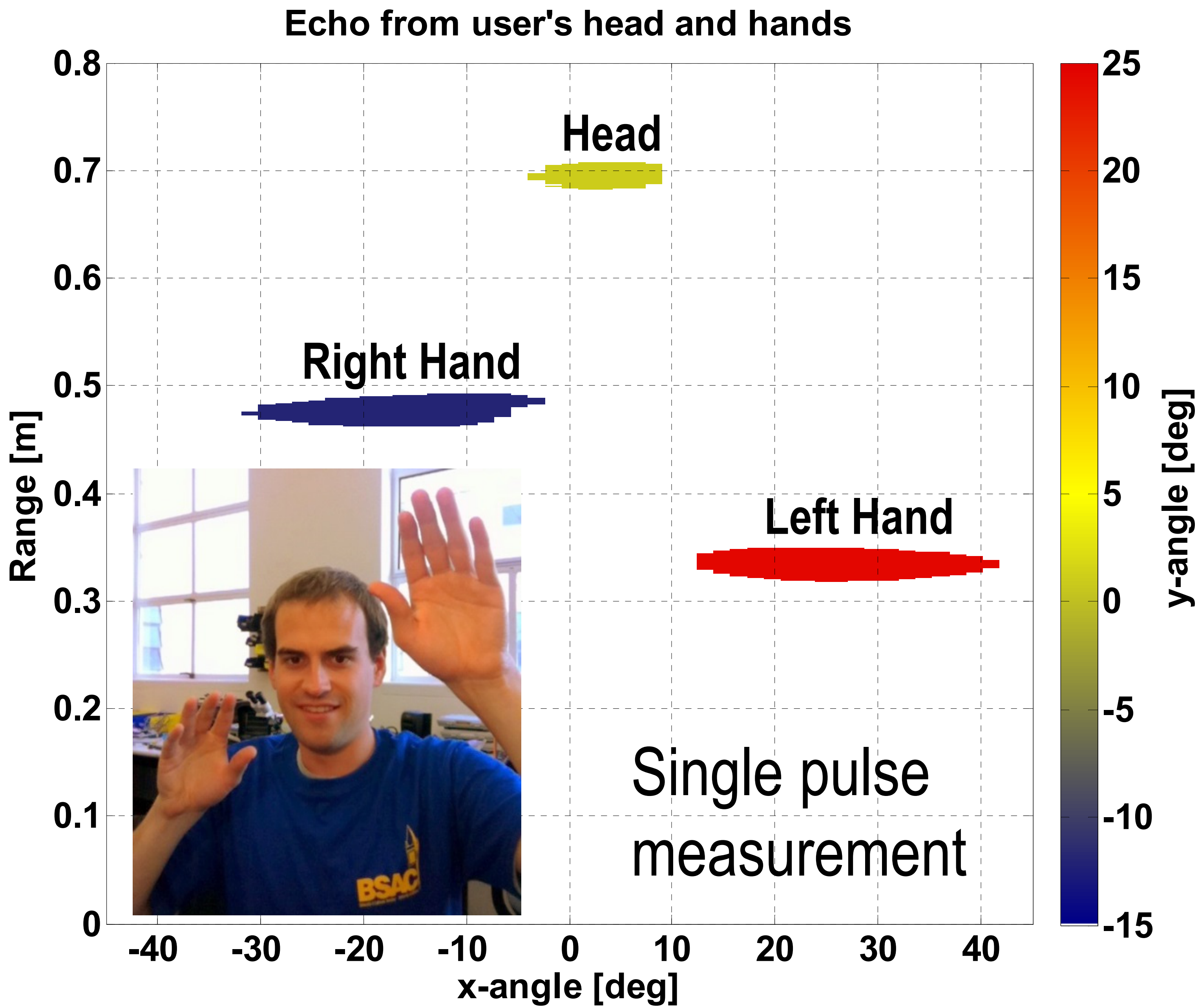
CMOS ASIC



10 channels
0.17mm^2 per ch.
0.18µm CMOS

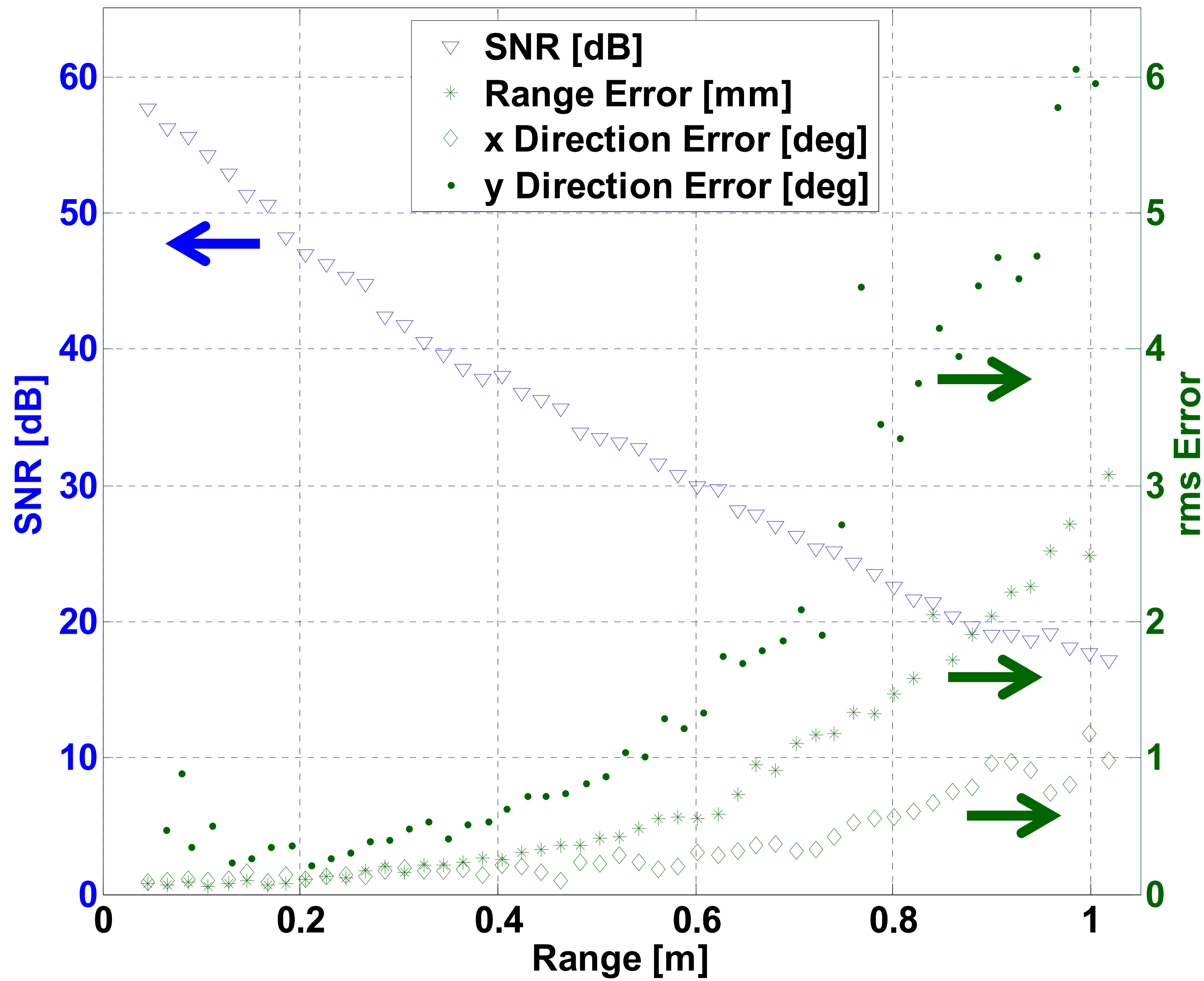
MEMS ultrasound chip



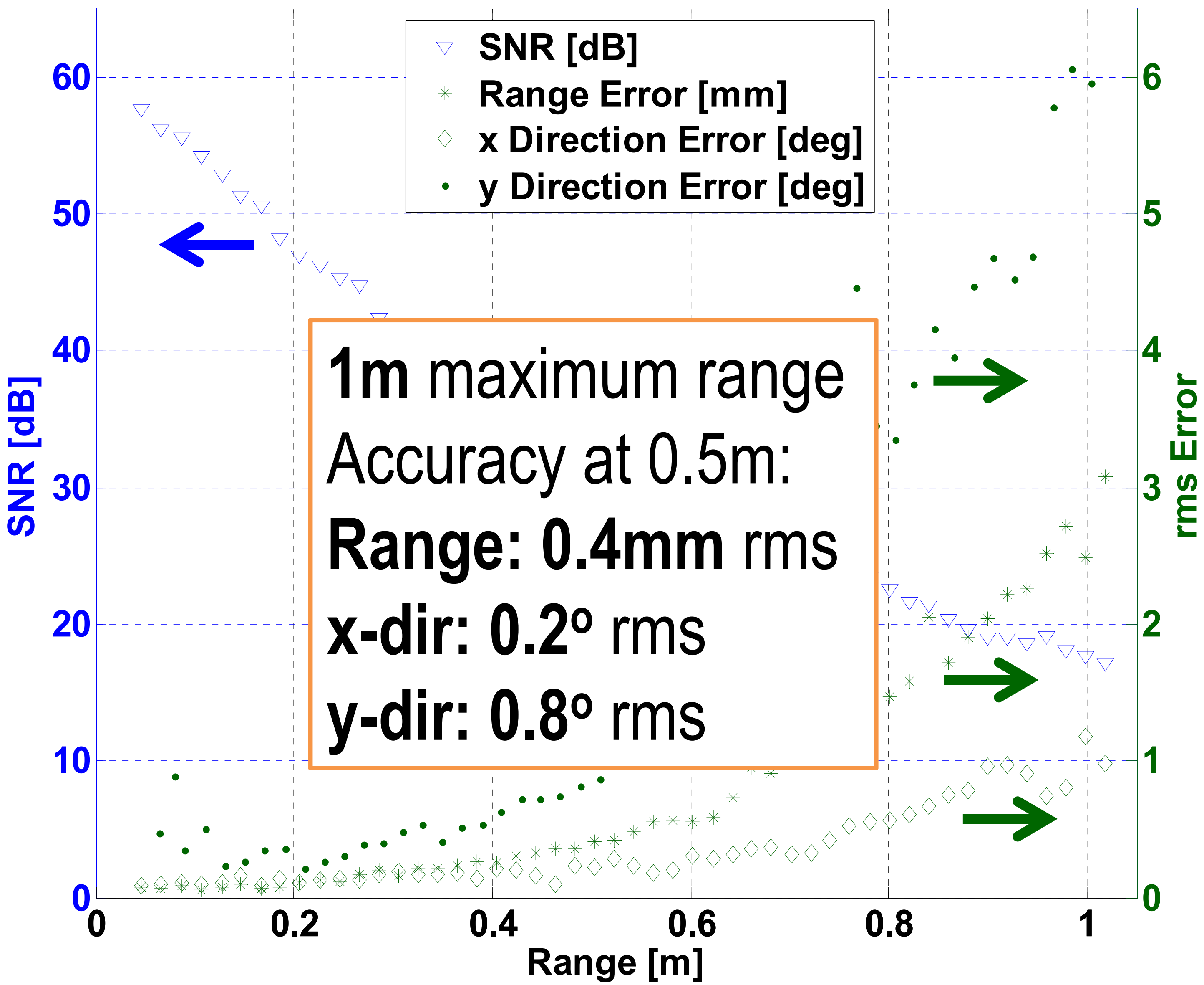


Echo from user's head and hands
Head
Right Hand
Left Hand
Single pulse measurement
Range [m]
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-40
-30
-20
-10
0
10
20
30
40
x-angle [deg]
25
20
15
10
5
0
-5
-10
-15
y-angle [deg]
BSAC

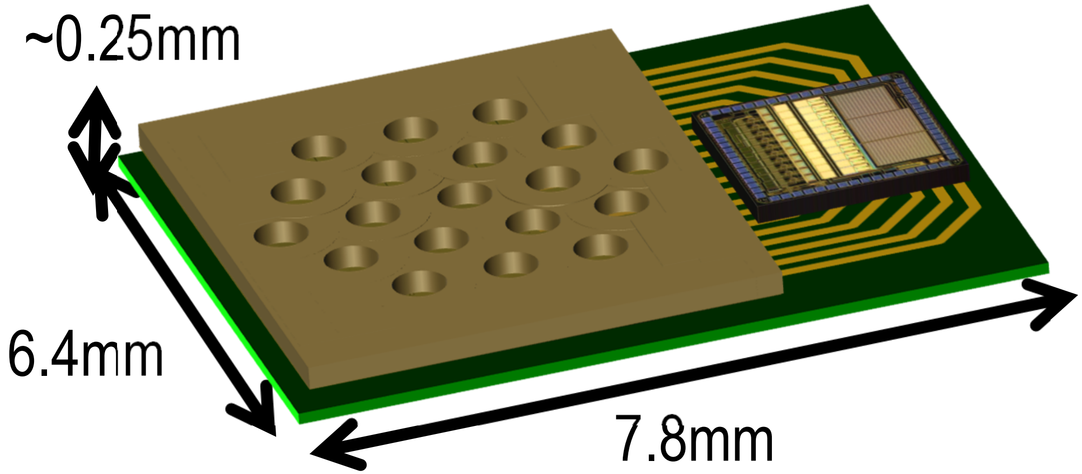
Random Range Error, Random Angle Error, and SNR vs. Range

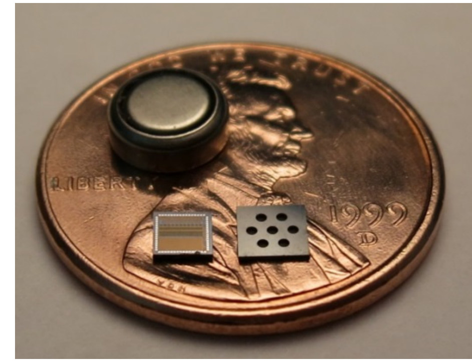


Random Range Error, Random Angle Error, and SNR vs. Range



System Size & Power Consumption



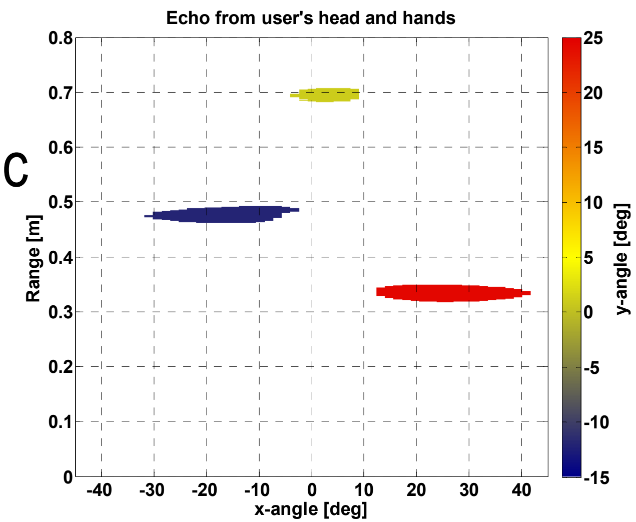


15mm³ solution volume

Power consumption (incl. estimated digital):
- **460µW (7 ch.) at 30fps w/ 1m max range**
- **10µW (1 ch.) at 10fps w/ 0.3m max range**

Conclusions

Demonstrated ultrasonic 3D rangefinding using 400µW CMOS readout IC



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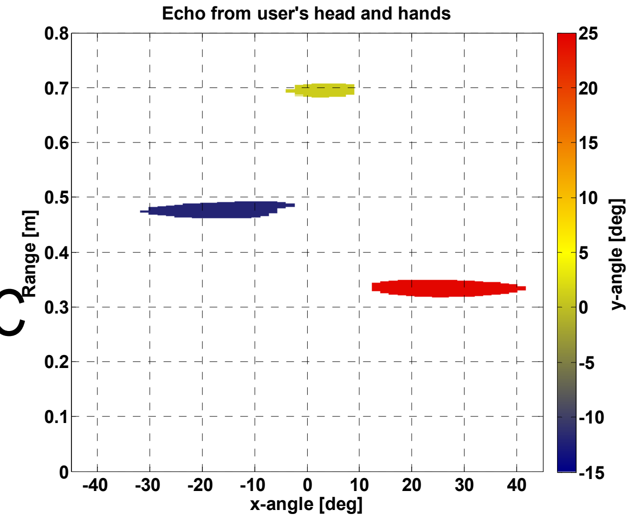
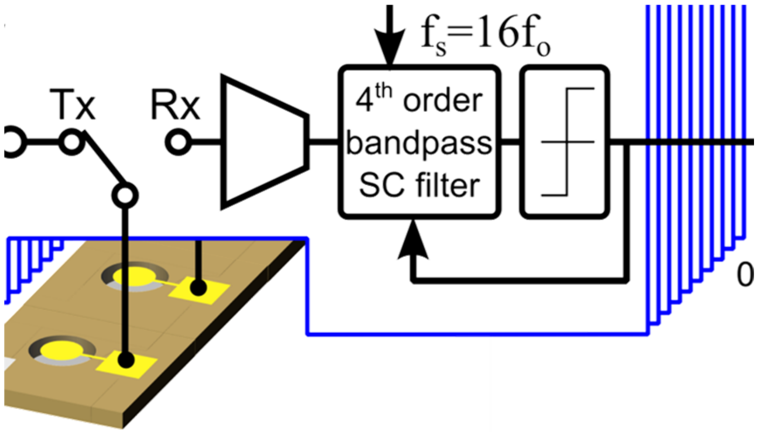
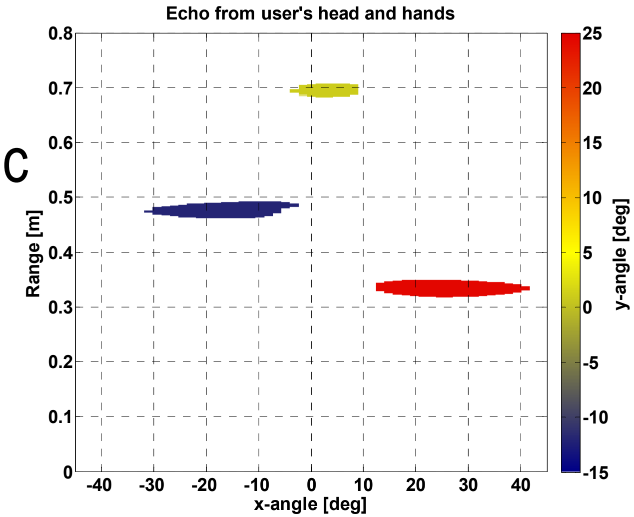


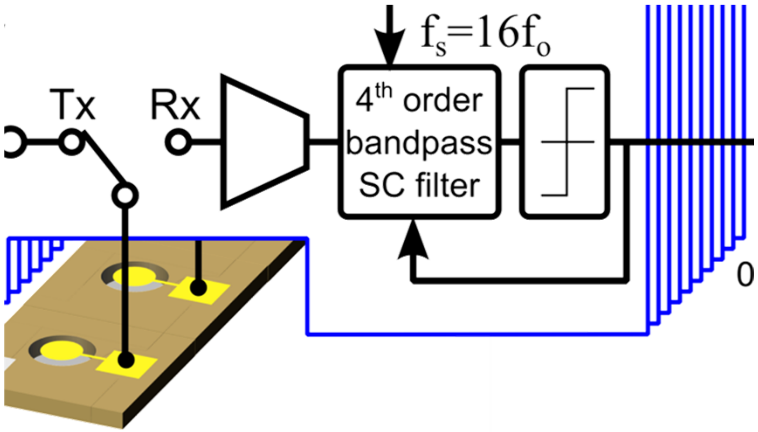


Mixed CT/SC architecture readout for noise efficiency

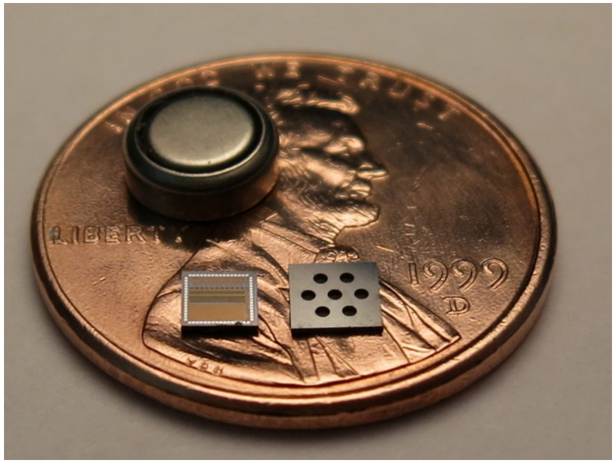
Conclusions

Demonstrated ultrasonic 3D rangefinding using 400μW CMOS readout IC





Mixed CT/SC architecture improves noise efficiency



Ultrasonic gesture recognition balances size, performance, and cost and can enable mm-sized gestural interfaces

3D Gesture Sensing System for Interactive Displays based on Extended-range Capacitive Sensing

Yingzhe Hu,

L. Huang, W. Rieutort-Louis, J. Sanz-Robinson,

S. Wagner, J. C. Sturm, N. Verma

Princeton University

Human-gesture Interfaces to Display

Applications for gesture sensing

Multi-use spaces (e.g., Tesla trip computer)

Visual computing

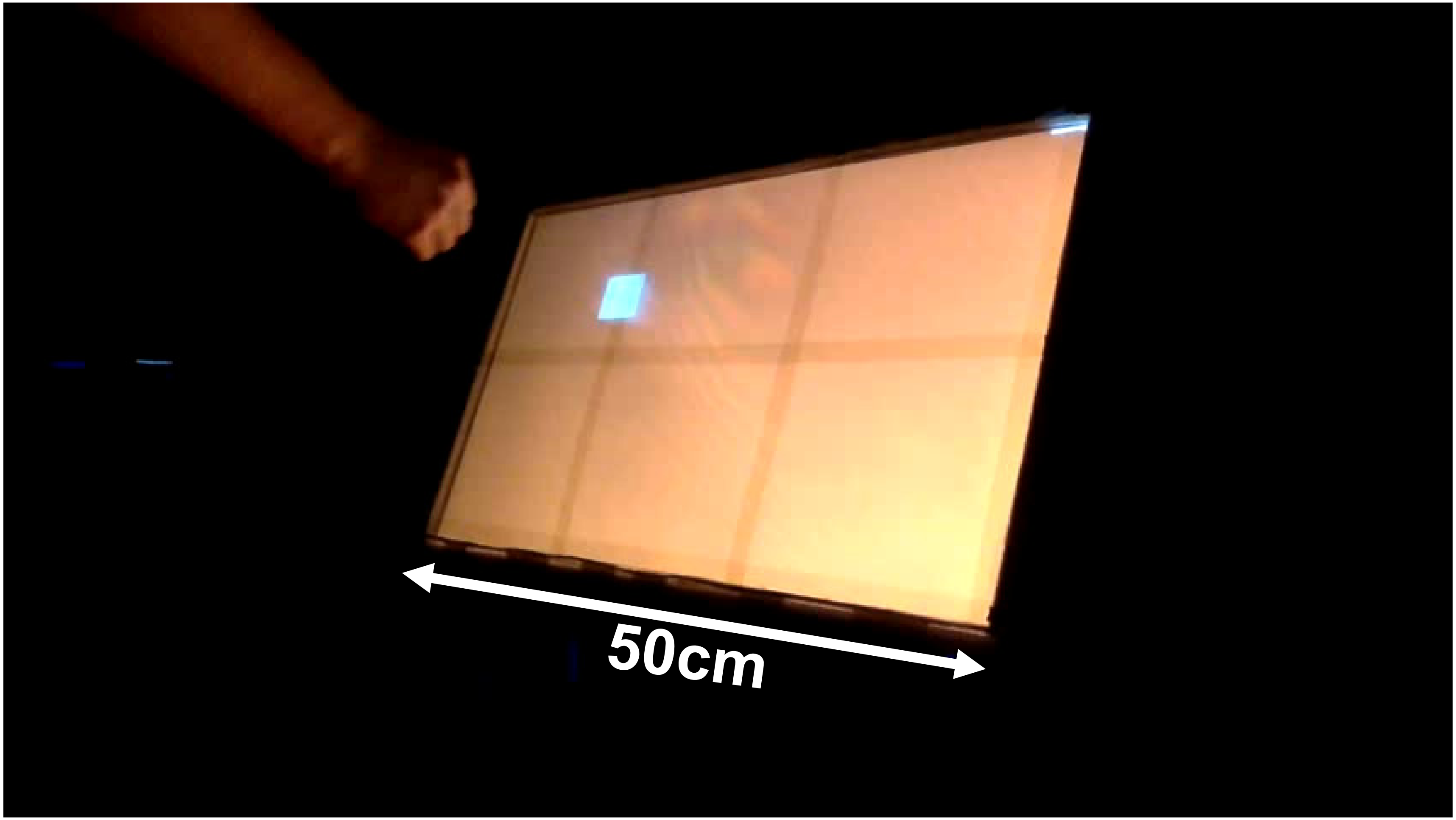
Large-scale displays & digital signage

Technologies for gesture sensing

Technology	Optical based	Capacitive sensing
Near-display detection	Poor	Strong
Power consumption	1-10W	<0.1W
Lighting condition	Light	None
Detection distance	meters	mm

Our aim: human-gesture interfacing (> 30cm) using low-power capacitive sensing, scalable to large displays

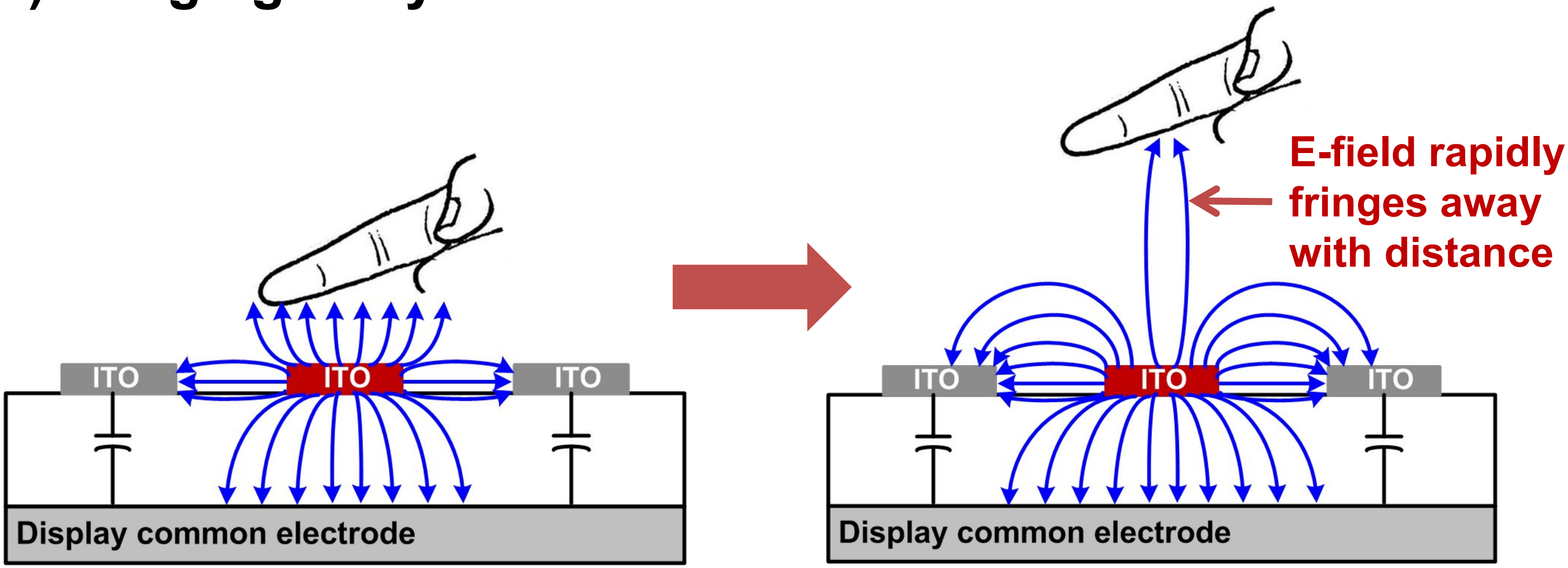
Display-integrated System
(from ISSCC demo session)



Presented by: Yingzhe Hu, Abigail Ward (algorithm)

Challenges of Extended-range Capacitive Sensing

(1) Fringing away of electric field:



Challenges of Extended-range Capacitive Sensing

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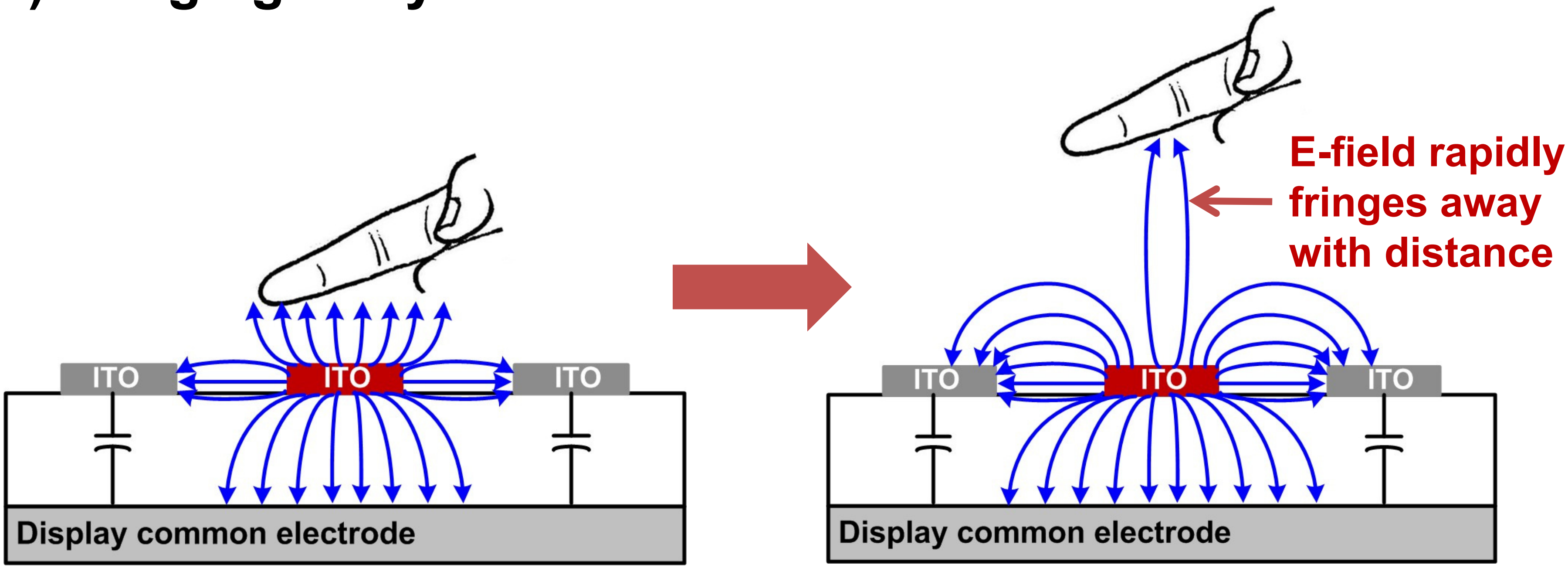
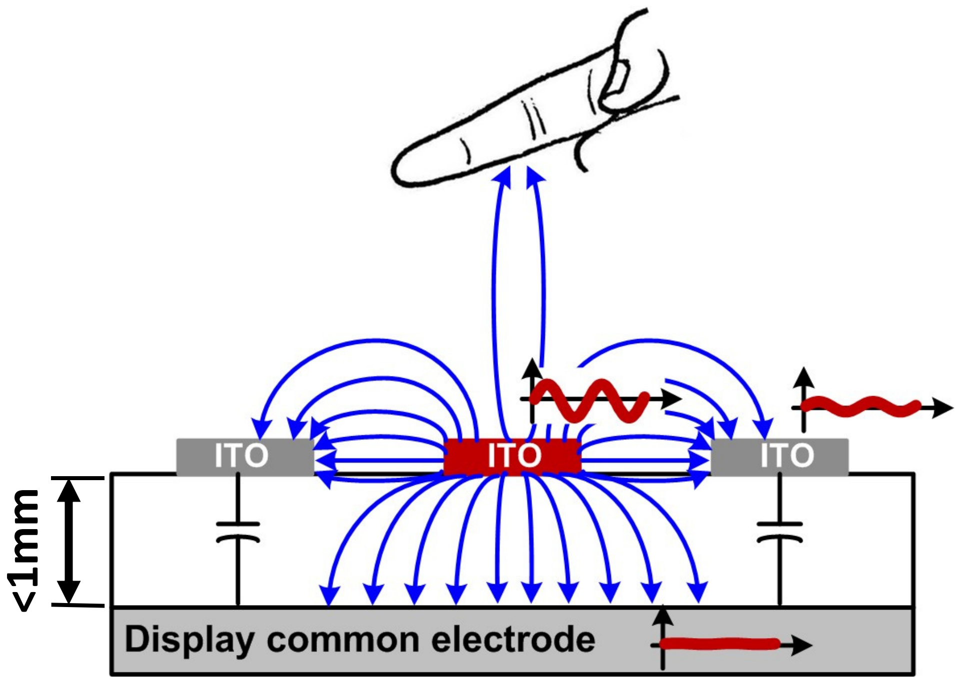


(2) Reduced capacitance due to increased distance:

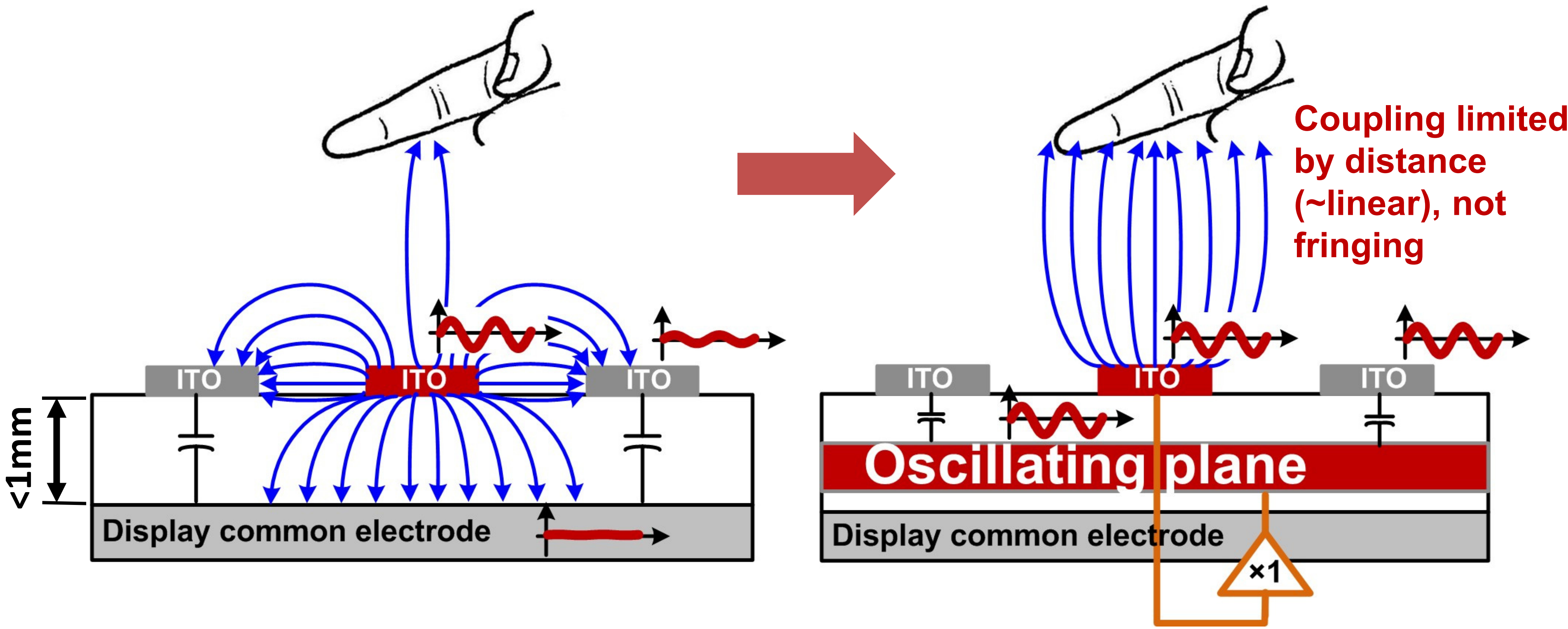
Parallel-plate approximation:

$$(\downarrow)\ C \approx \frac{\varepsilon_0 A}{d\ (\uparrow)}$$

Minimizing Electric-field Fringing



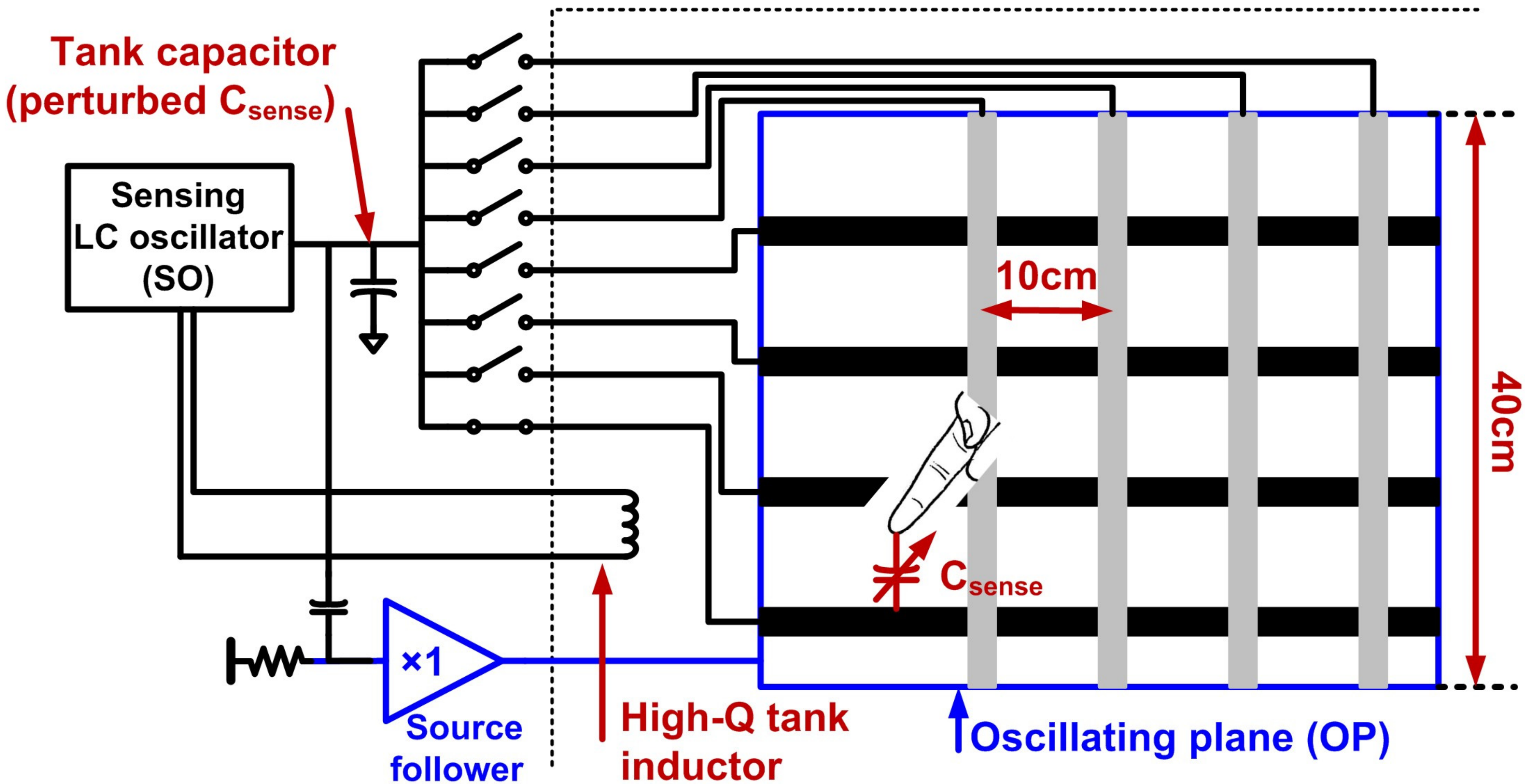
Minimizing Electric-field Fringing



Surrounding features actively driven to potential of sensing electrode

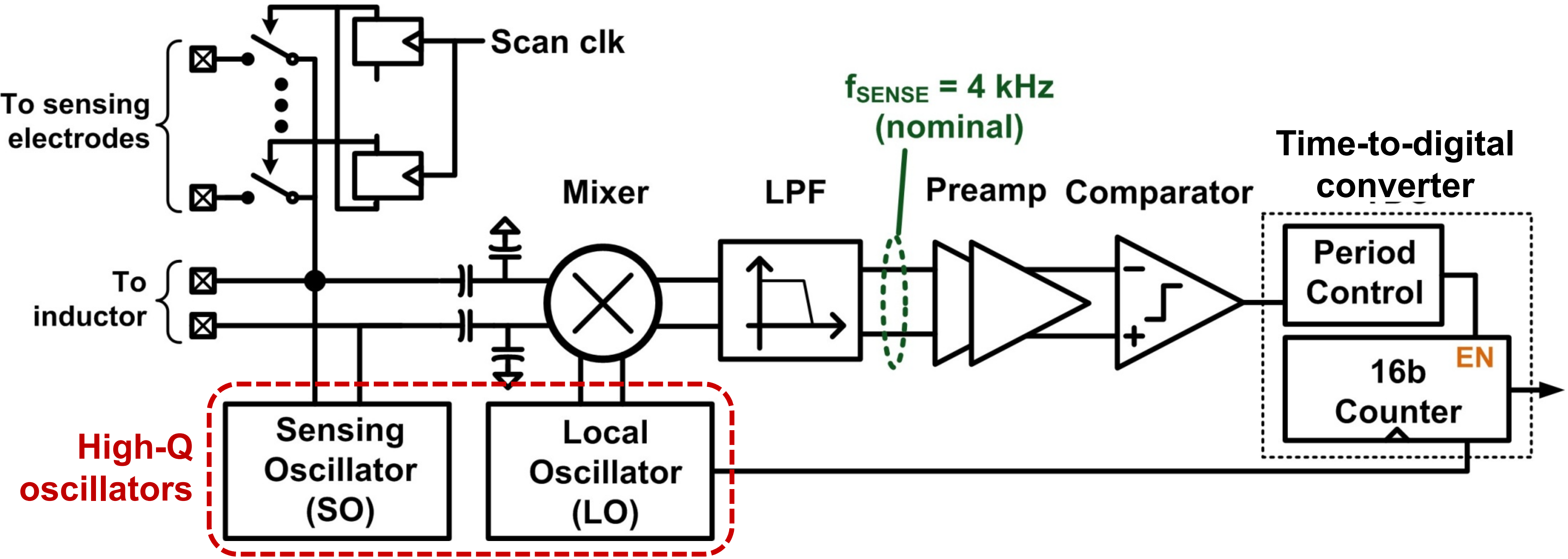
Oscillating plane (OP) eliminates capacitance fringing

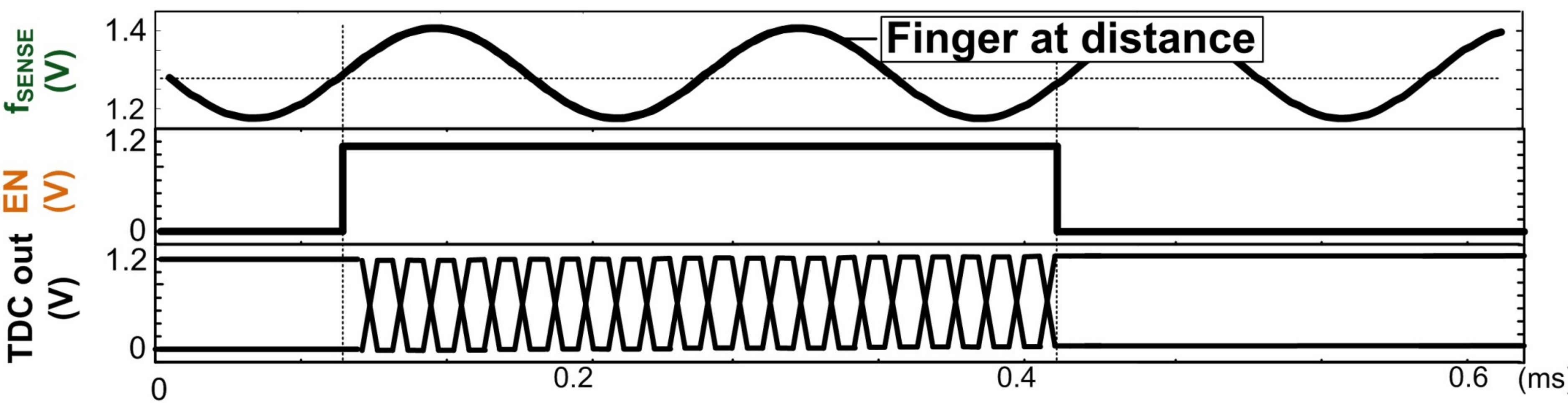
System Architecture: Cap-to-freq Readout



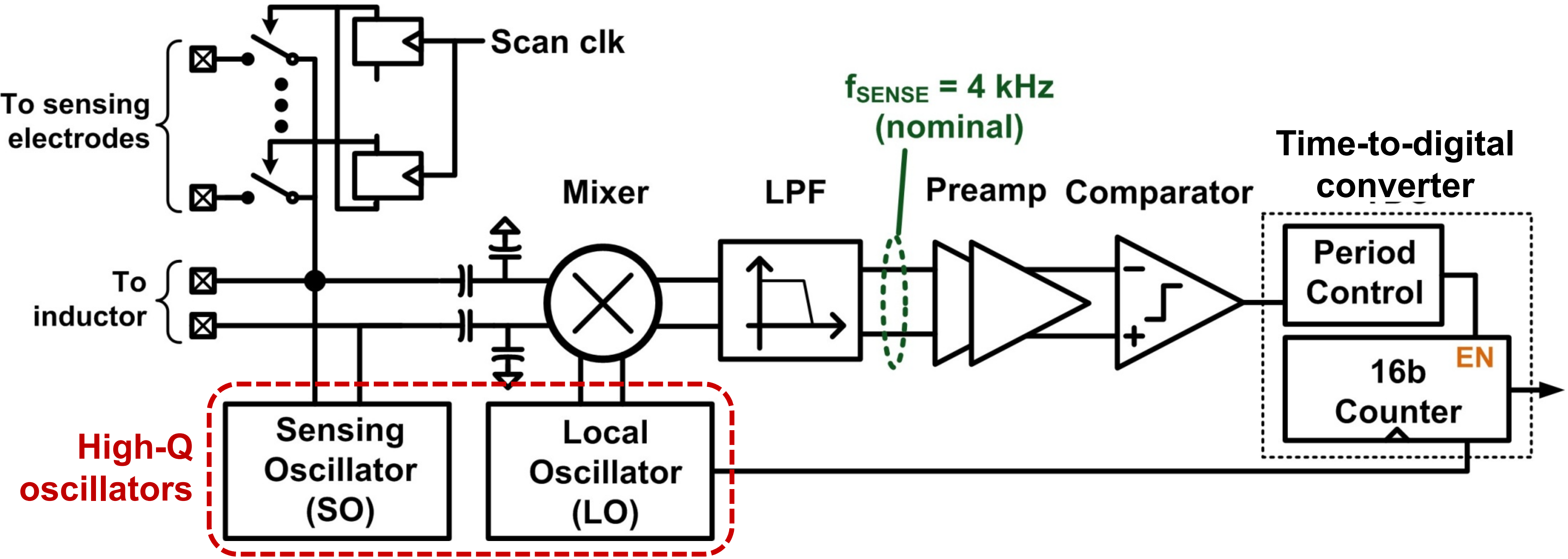
1) Sensitivity enhanced by high-Q sensing oscillator
2) Small number of electrodes (4+4) thanks to extended-range

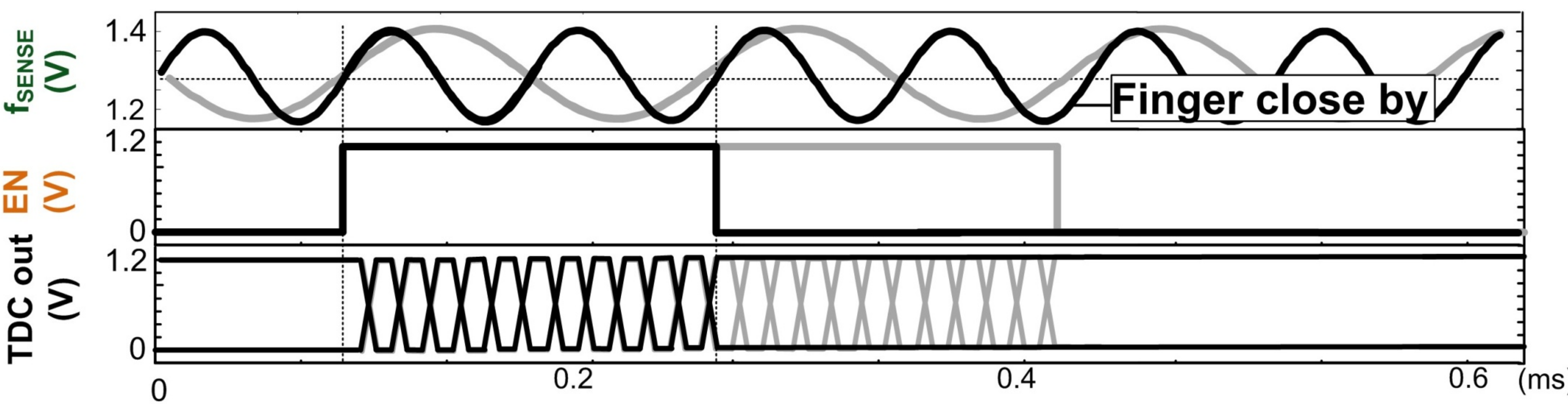
Sensing Readout Channel Architecture



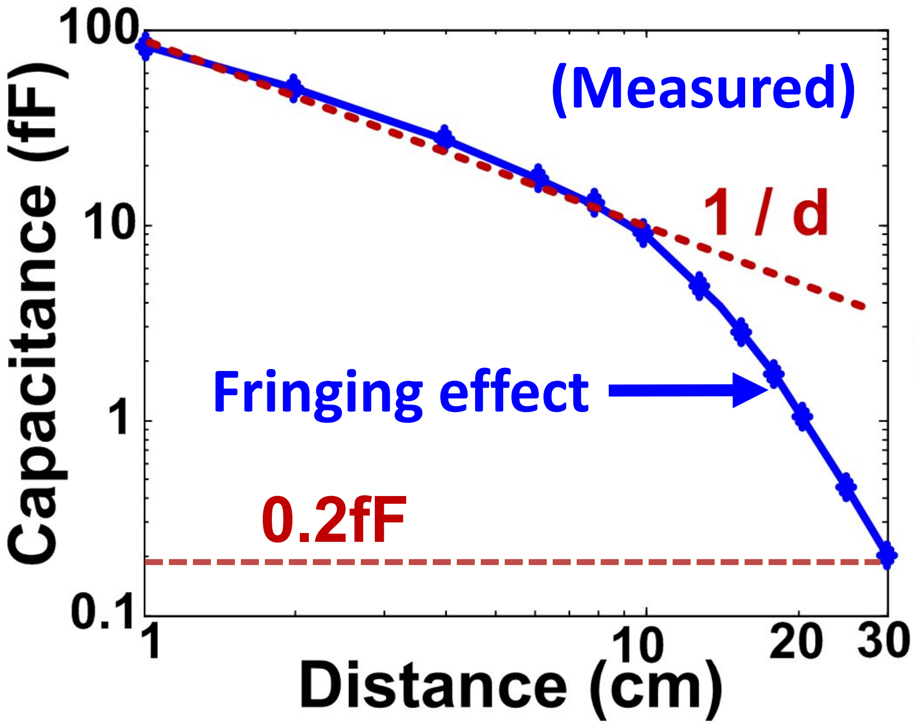


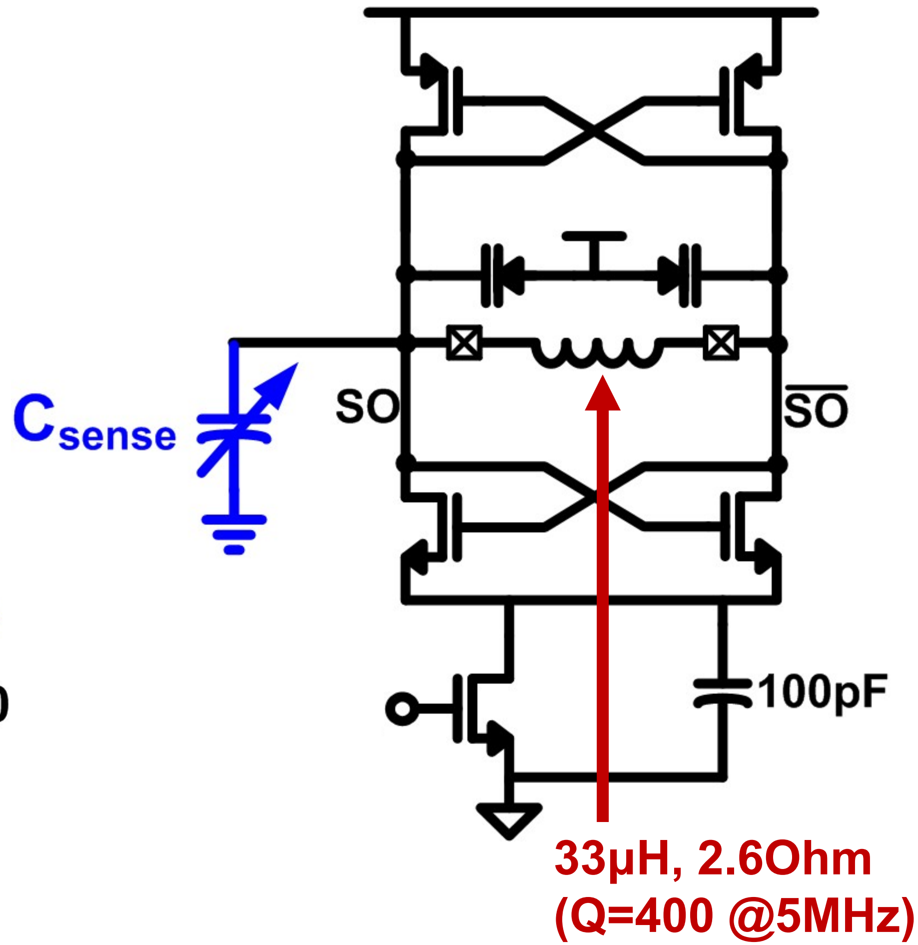
Sensing Readout Channel Architecture





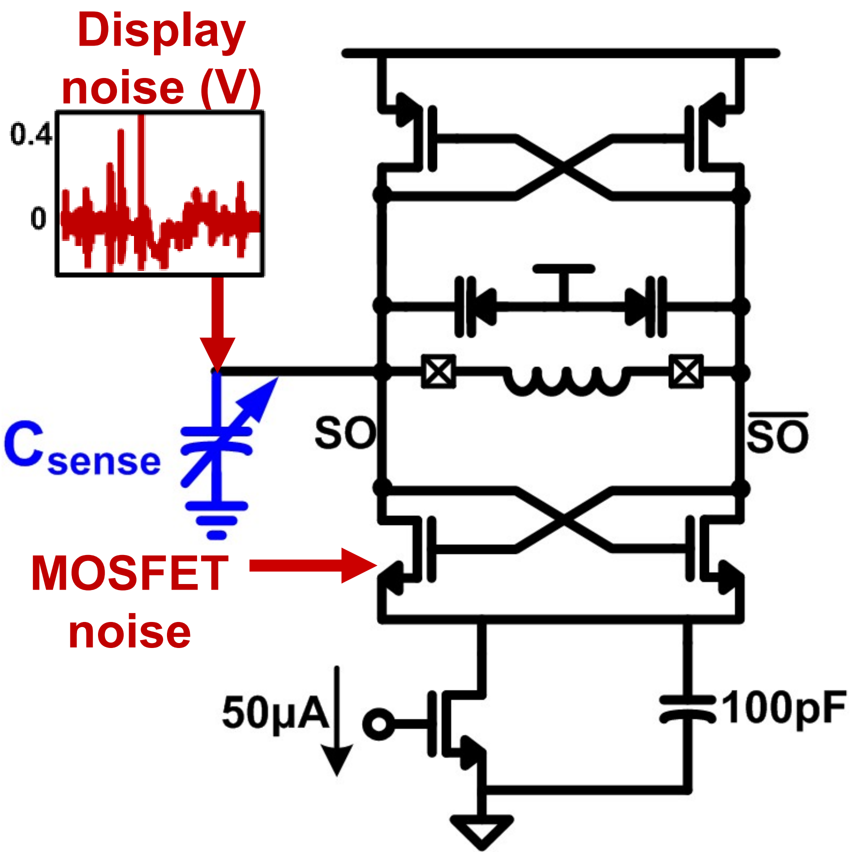
Sensing LC Oscillators

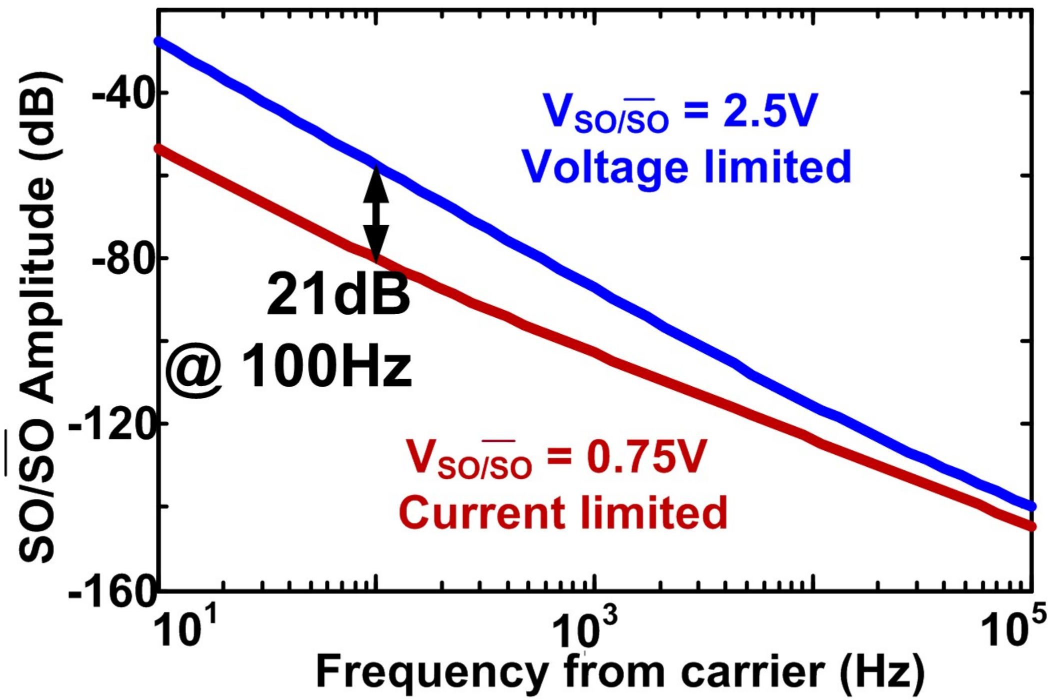




Sensing tiny capacitance requires oscillator with high frequency selectivity → Use high-Q tank inductor

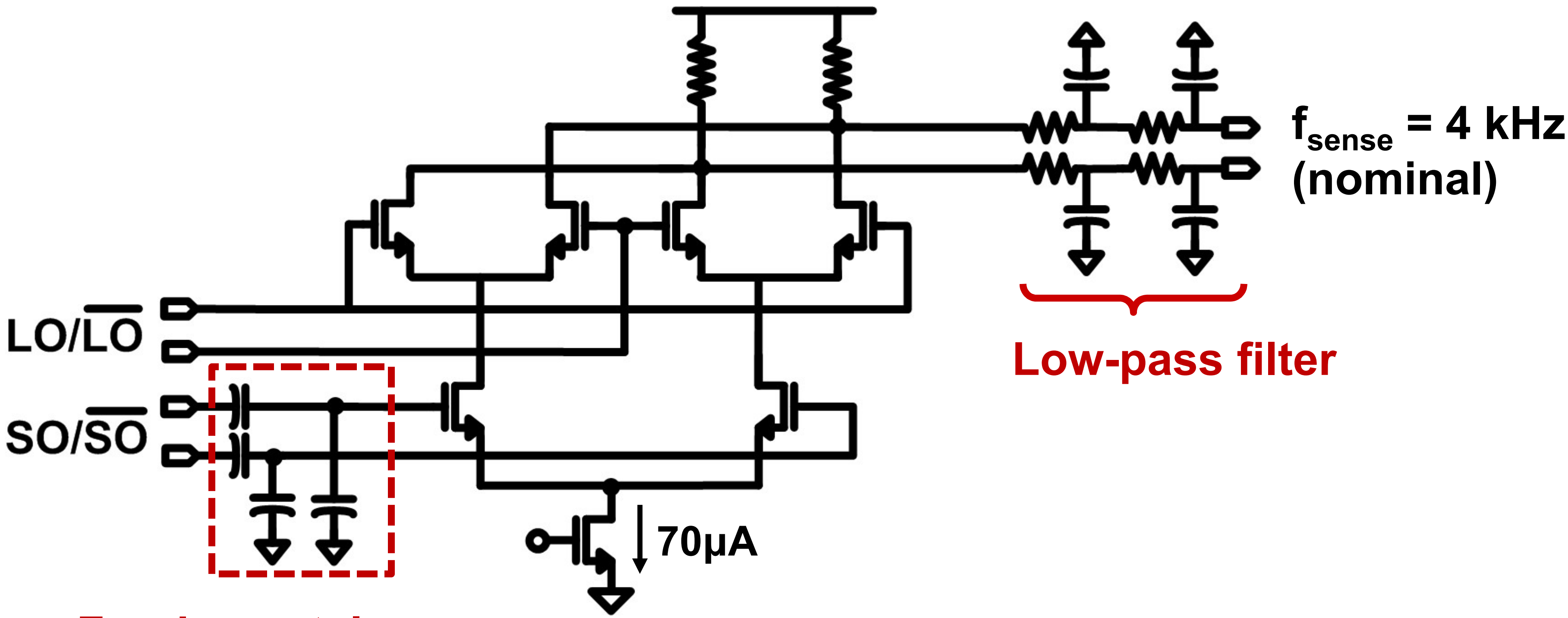
Sensing LC Oscillators

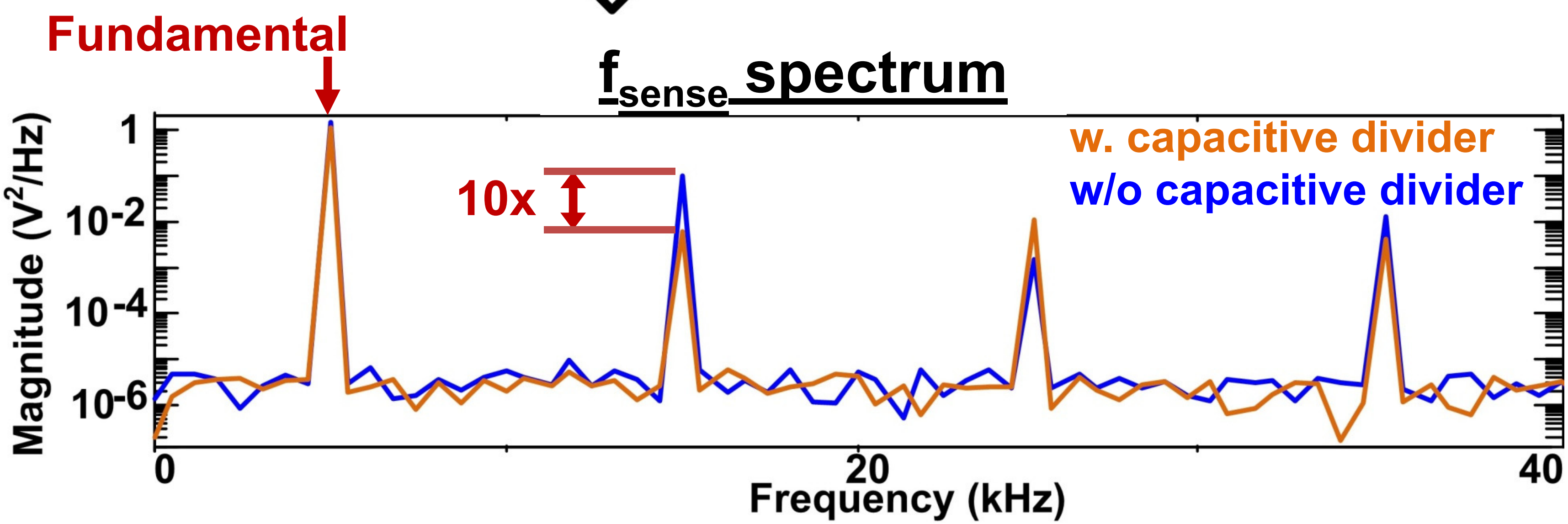




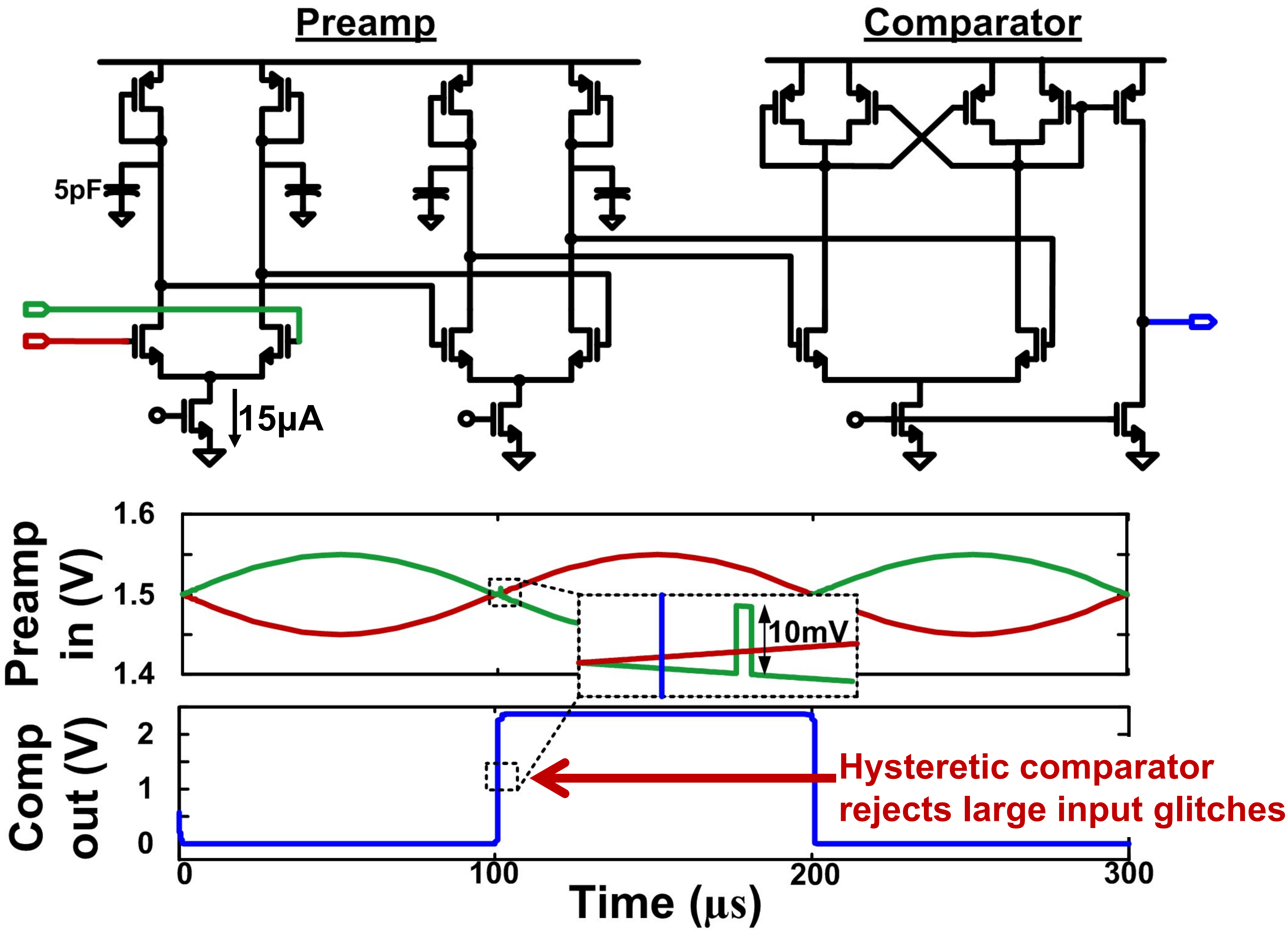
Current-limited biasing to balance noise from transistors and noise from stray coupling (display)

Gilbert Mixer: Cap. Divider for Linearity

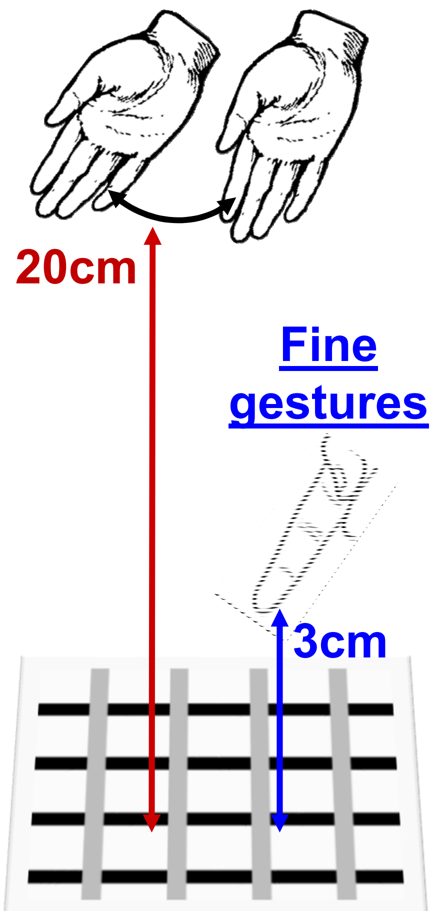




Preamp and Comparator



TDC for Z-directional SNR Enhancement



Δx = 1cm

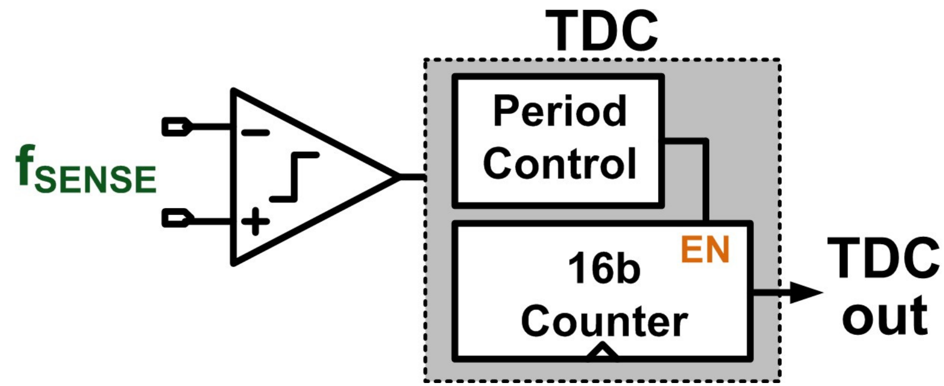
Δf = 24Hz

***f**$_{SENSE}$* **= 4.11 kHz**

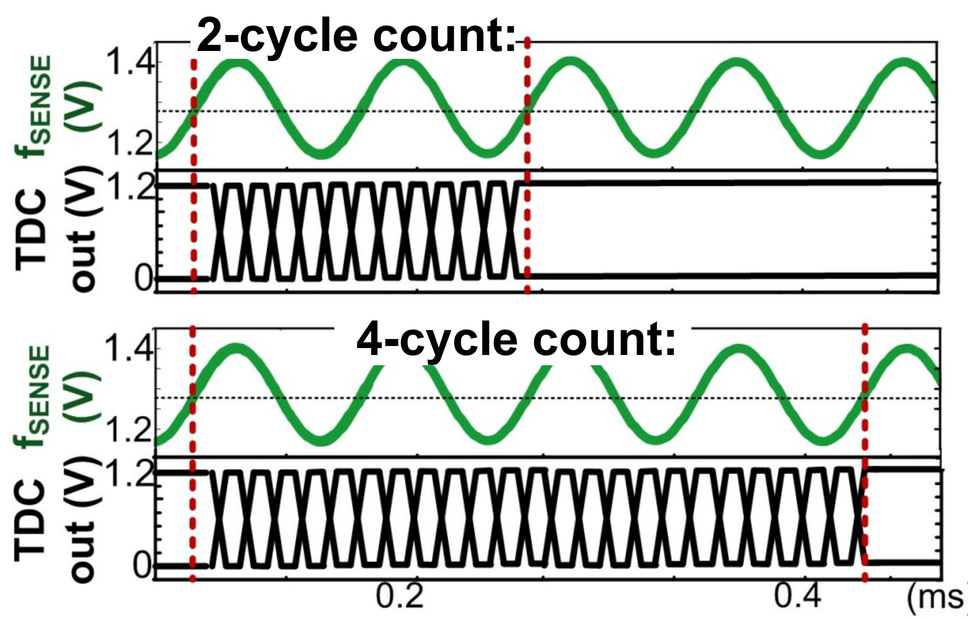
Δx = 1cm

Δf = 870Hz

***f**$_{SENSE}$* **= 8.1 kHz**

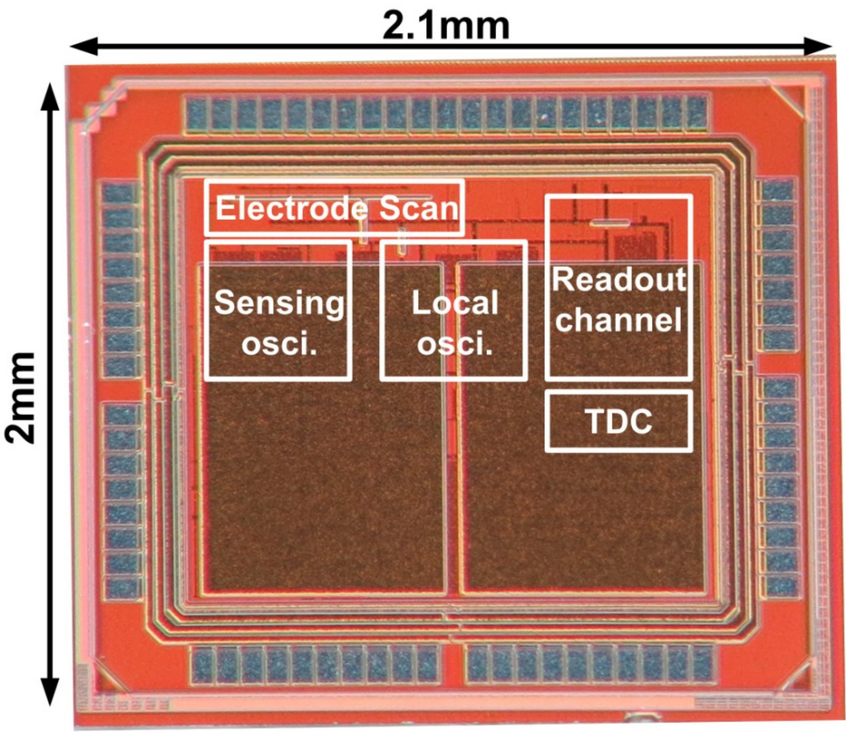


Enables counting over multiple cycles:

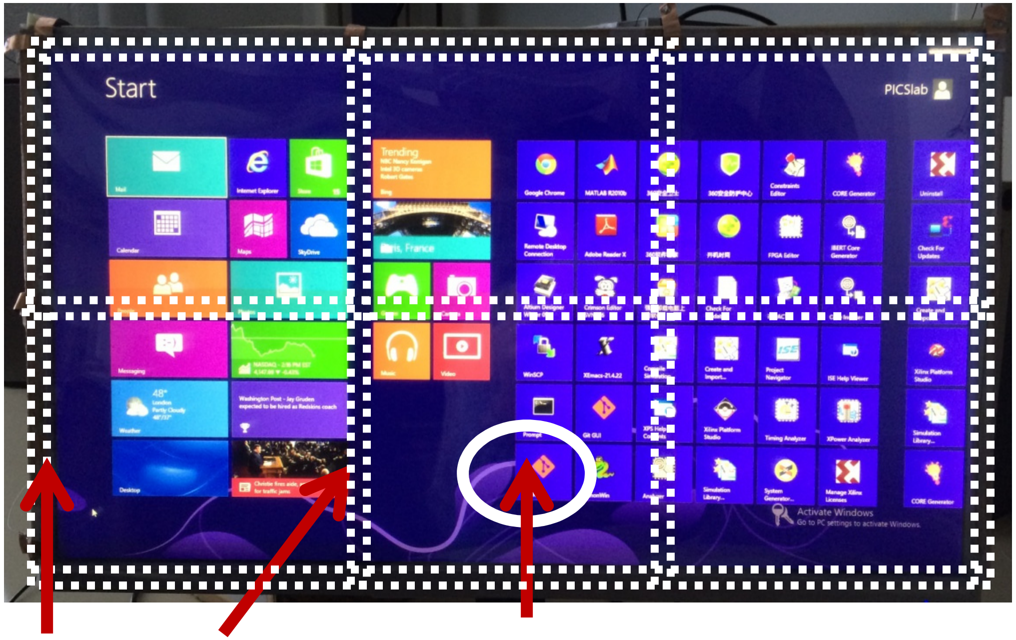


Close-in resolution enhanced thanks to increased capacitance change *and more averaging over f$_{SENSE}$ cycles*

System Prototype



Display-integrated Demonstration



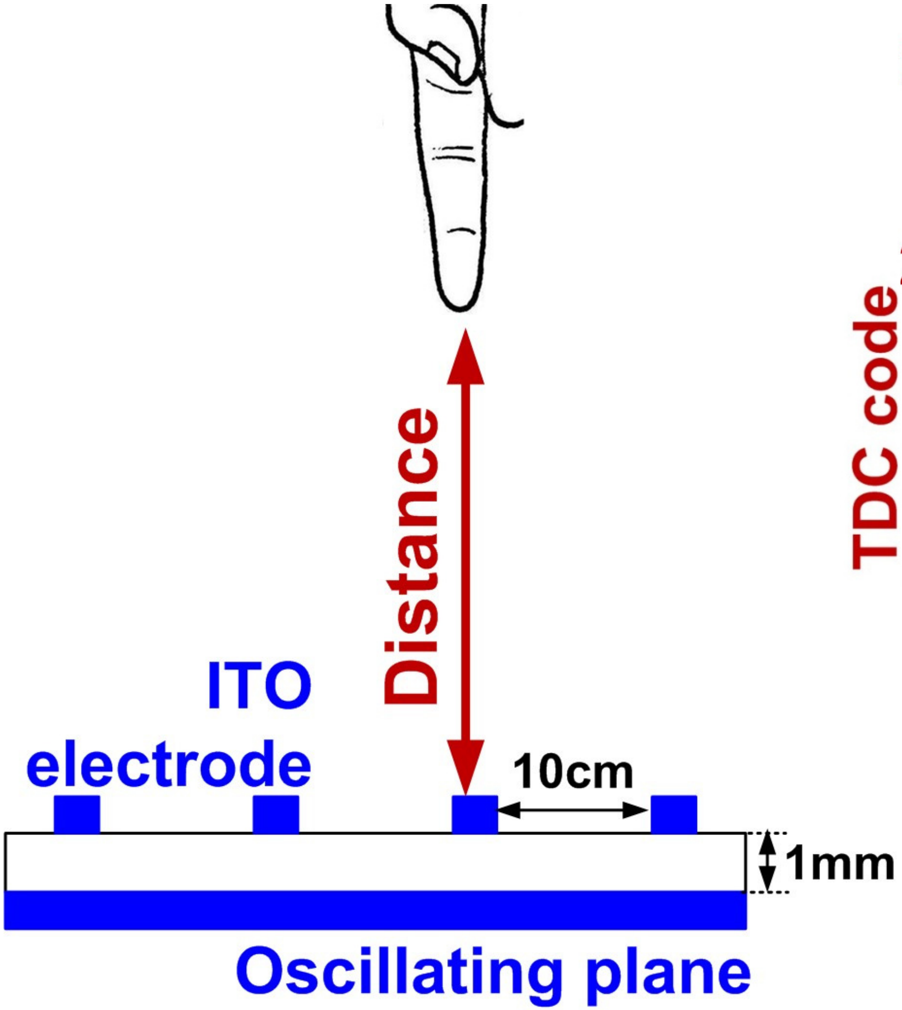
ITO Sensing electrodes

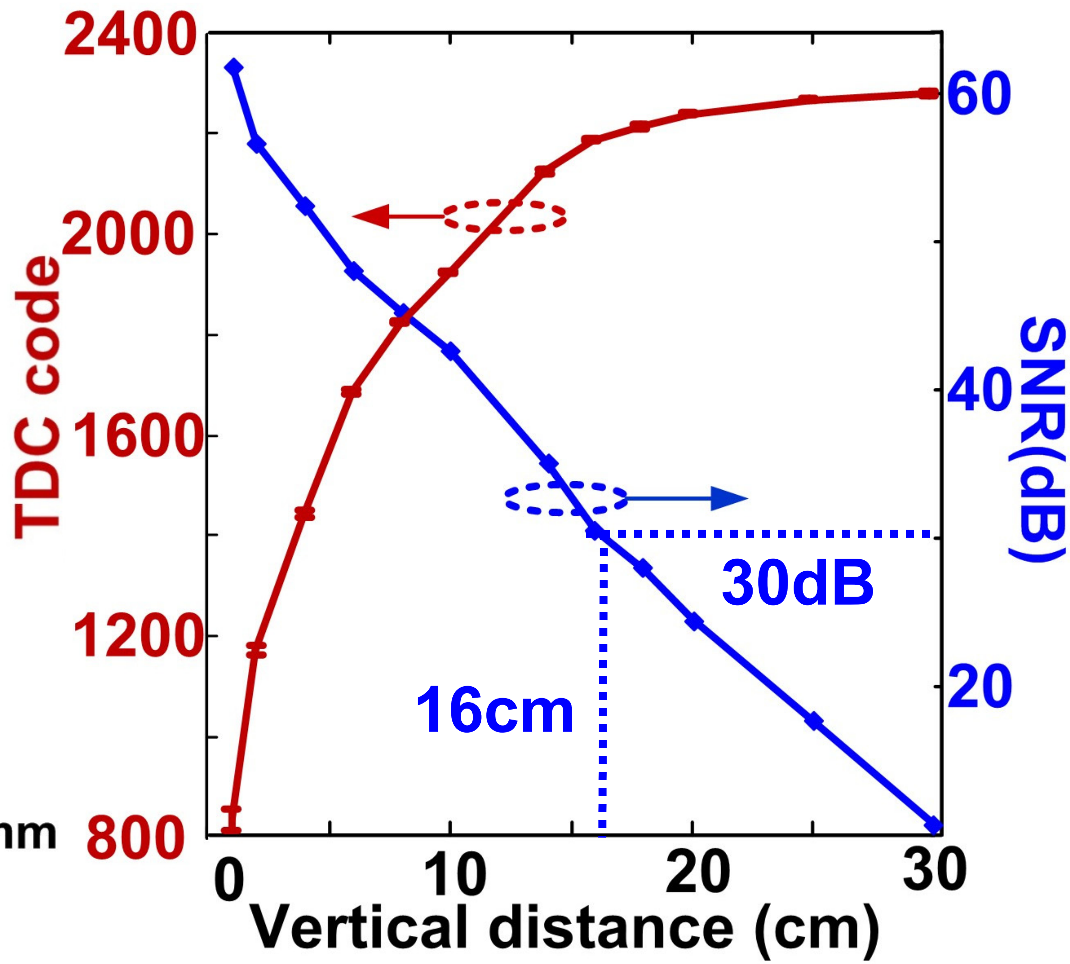
ITO Oscillating plane

Performance Summary:

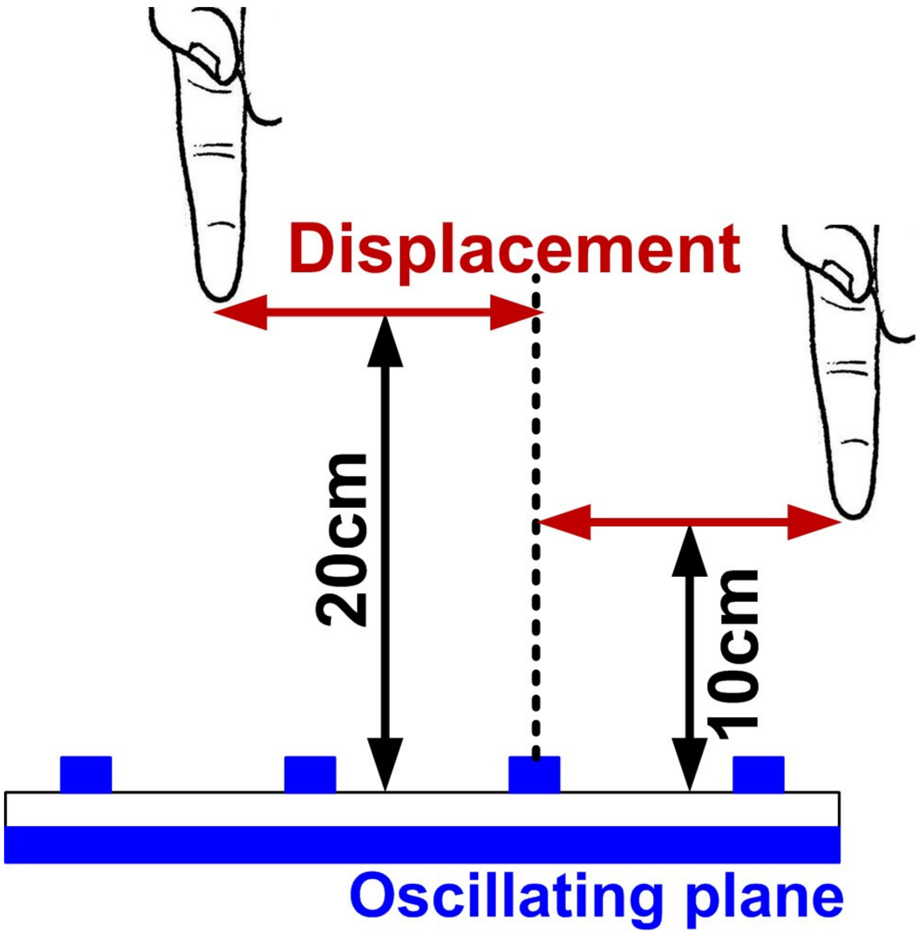
Process	Channels	Scan rate	SNR	Power
1.2/2.5V 130nm	8 (X+Y)	240Hz	30dB @16cm	475μW (readout) 19mW (OP)

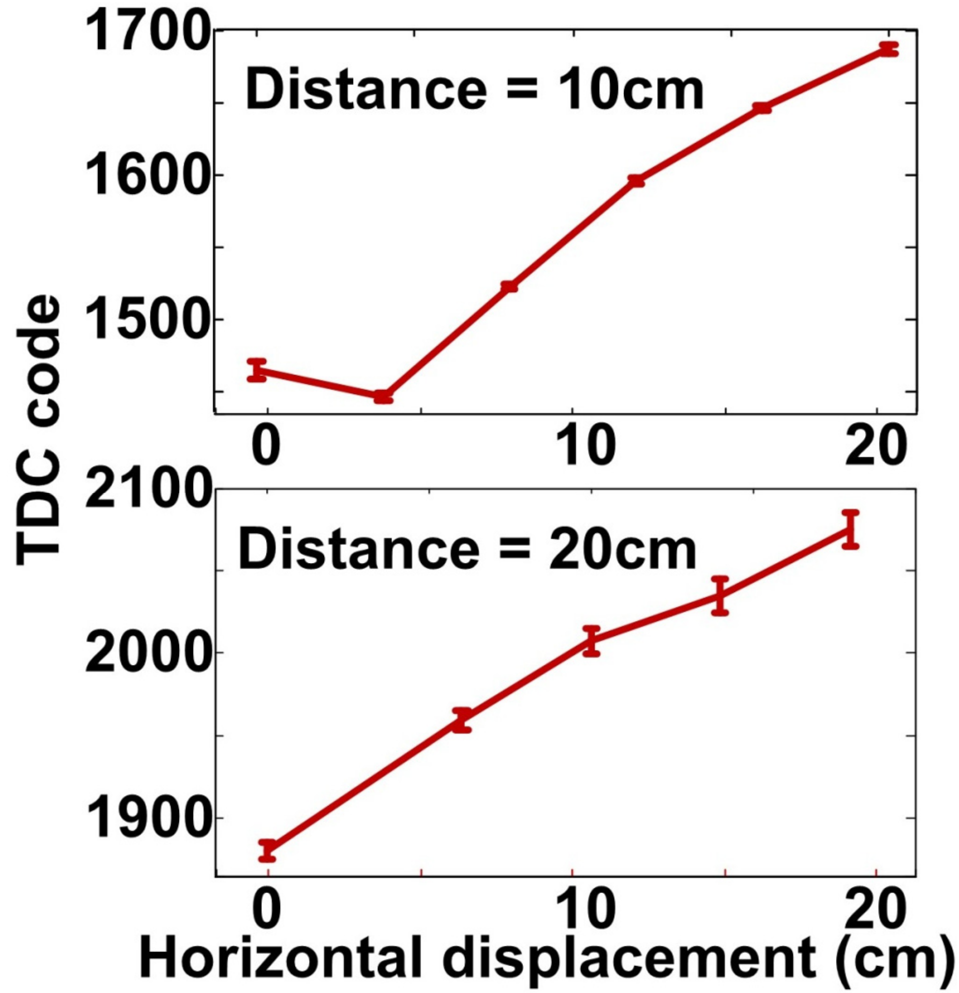
Measurement Results : Vertical





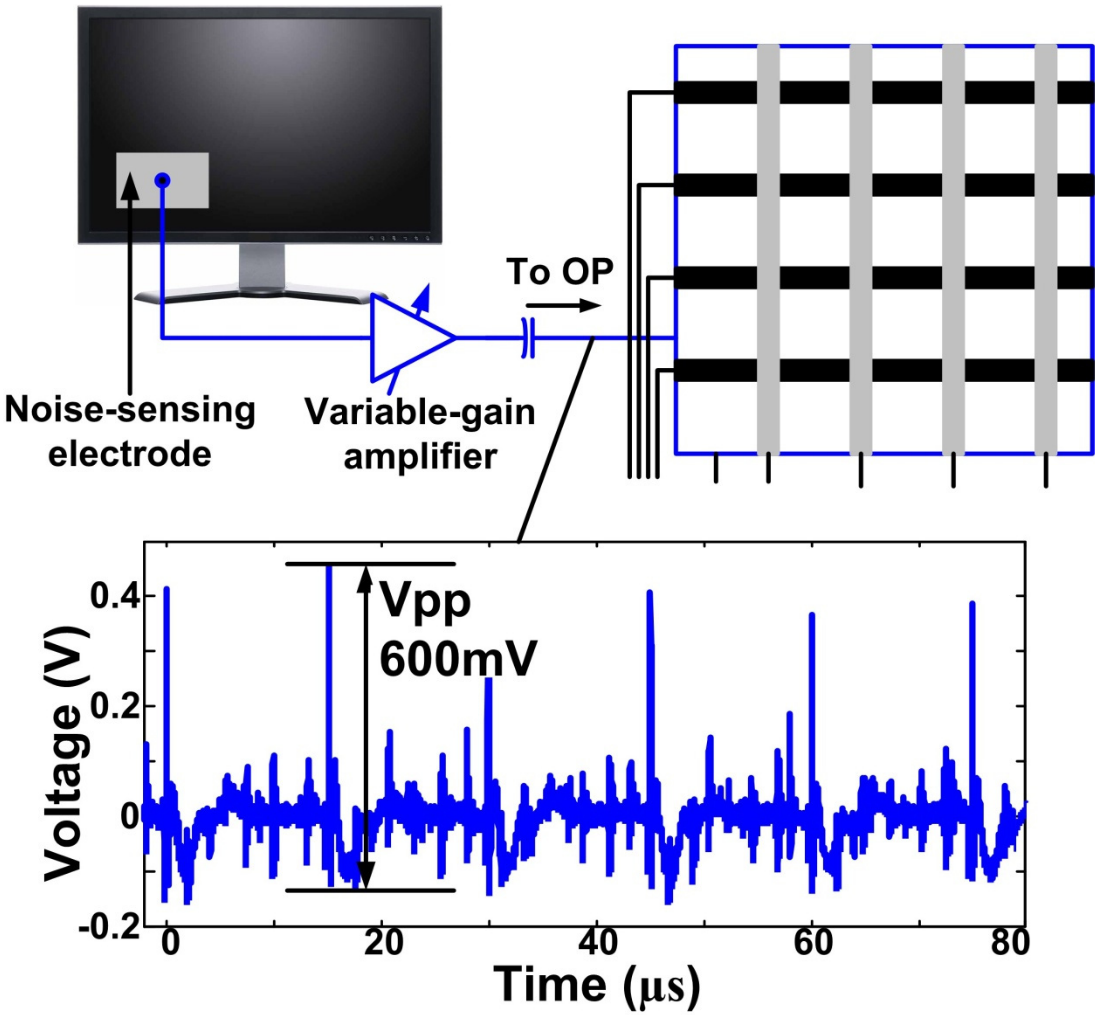
Measurement Results: Horizontal

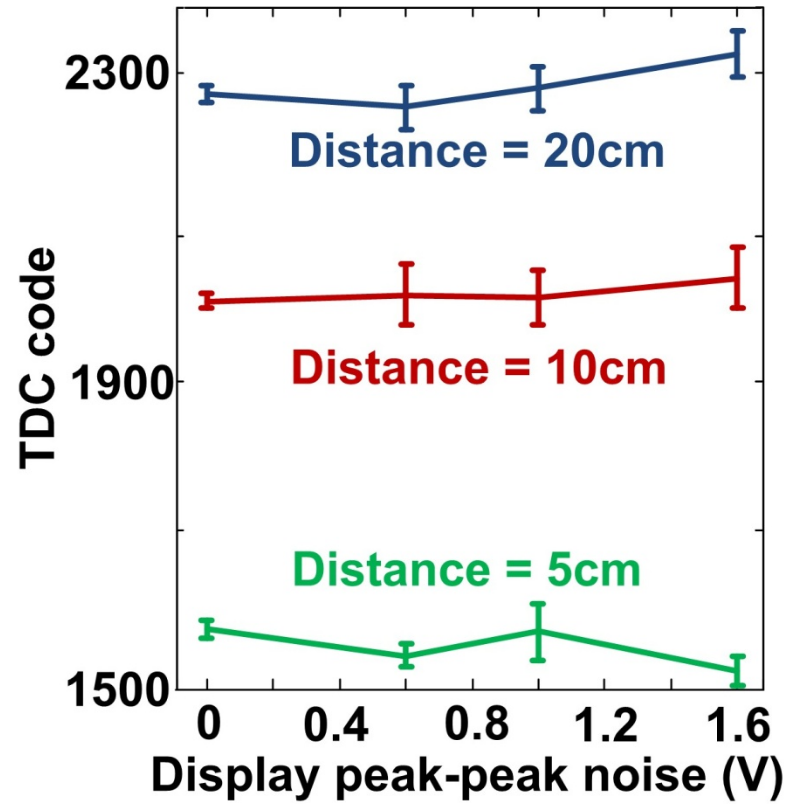




Horizontal resolution of 7.1mm @20cm distance

Display Noise Measurements





Large display noise is substantially rejected by OP shielding and high-Q filtering in frequency readout

Conclusions

- Extended-range capacitance sensing achieved by:
  1. Oscillating plane directing sensing-electrode's E-field away from surround electrodes
  2. High-Q oscillator enabling increased frequency selectivity for reduced capacitance at distances
- Extended-range sensing enables resolution with fewer electrodes for low-power readout
- Variable gesturing-sensing SNR possible for improving ergonomics

Acknowledgements: This work is partially funded by NSF and Qualcomm Innovation Fellowship. We thank MOSIS for IC fab.

A 240Hz-Reporting-Rate 143×81 Mutual-Capacitance Touch-Sensing Analog Front-End IC with 37dB SNR for 1mm-Diameter Stylus

Mutsumi Hamaguchi,

Akira Nagao,

Masayuki Miyamoto

Sharp Corporation, Japan

Outline of presentation

1. Motivation and background
2. Architecture
3. Verification
4. Summary

Outline of presentation

1. Motivation and background

2. Architecture

3. Verification

4. Summary

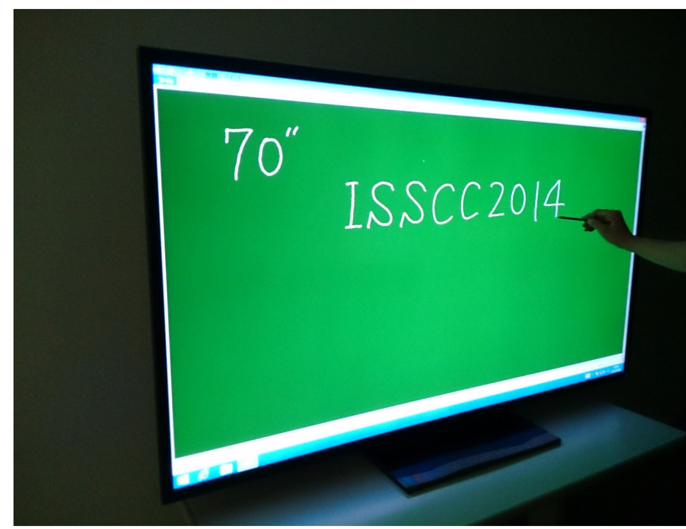
Motivation and background

Realization of mutual capacitance touch sensing systems with

1. Unified touch UI for all size of displays from 4-inch up to 100-inch,

2. Fine pen handwriting without additional pen digitizer,

3. Strong immunity against LCD noise.



Outline of presentation

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Architecture

1. Parallel Drive

✓ Properly designed parallel drive sequences enhance the SNR.

2. Fully differential sensing scheme

✓ LCD noise commonly injected into adjacent channels is cancelled.

✓ Capacitance change signals are solely detected.

Architecture

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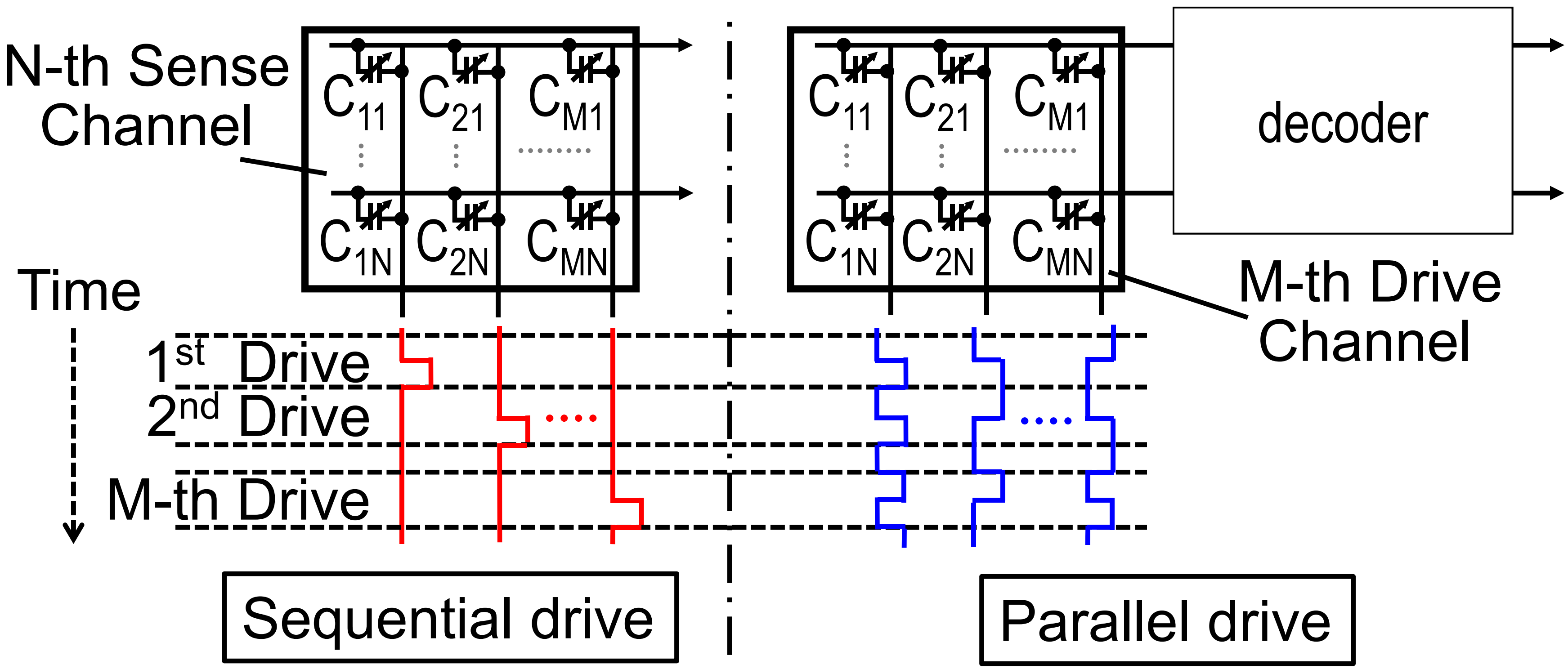
Sequential drive vs. Parallel drive



$$\text{out} \propto (C_{ij} + \text{noise}) \Rightarrow \text{out} \propto \left(M \bullet C_{ij} + \sqrt{M} \bullet \text{noise} \right)$$

$$\boxed{\text{SNR} : \times\sqrt{M}}$$

Architecture

1. Parallel Drive

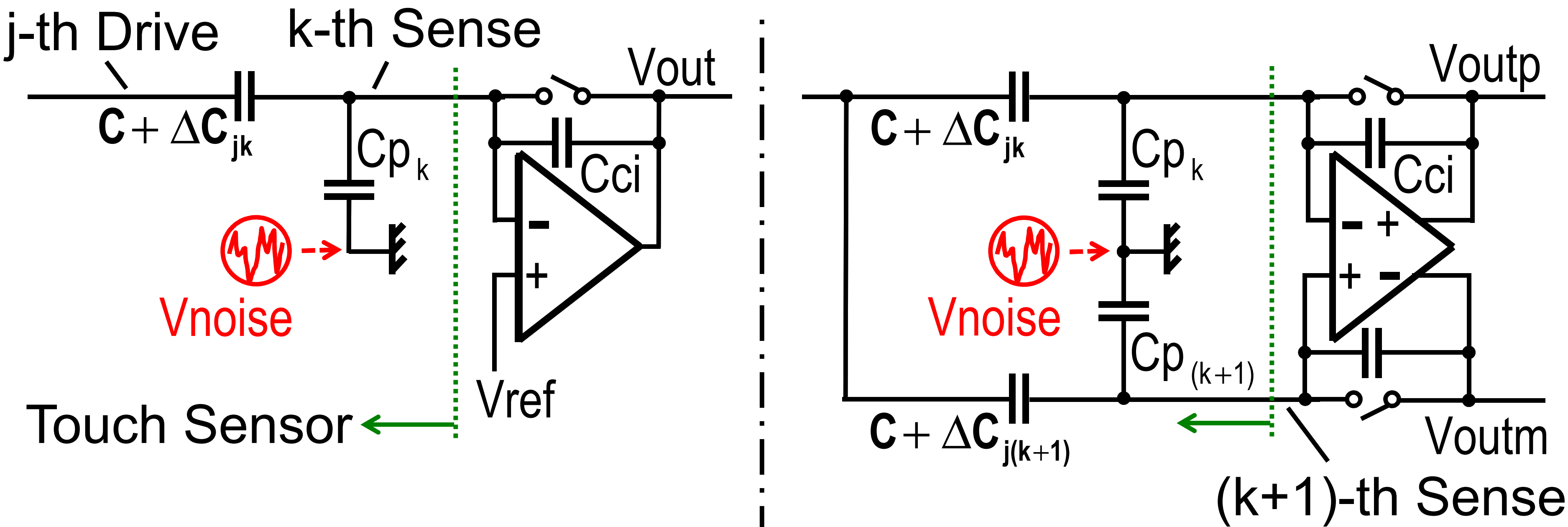
✓ Properly designed parallel drive sequences enhance the SNR.

2. Fully differential sensing scheme

✓ LCD noise commonly injected into adjacent channels is cancelled.

✓ Capacitance change signals are solely detected.

Single-ended vs. Differential



$$(1)\quad \mathbf{Vout} \propto \frac{(\mathbf{C} + \Delta\mathbf{C}_{jk})\bullet \mathbf{Vd} + \mathbf{Cp}_k \bullet \mathbf{Vnoise}}{\mathbf{Cci}}$$

if $\mathrm{Cp}_k = \mathrm{Cp}_{(k+1)}$

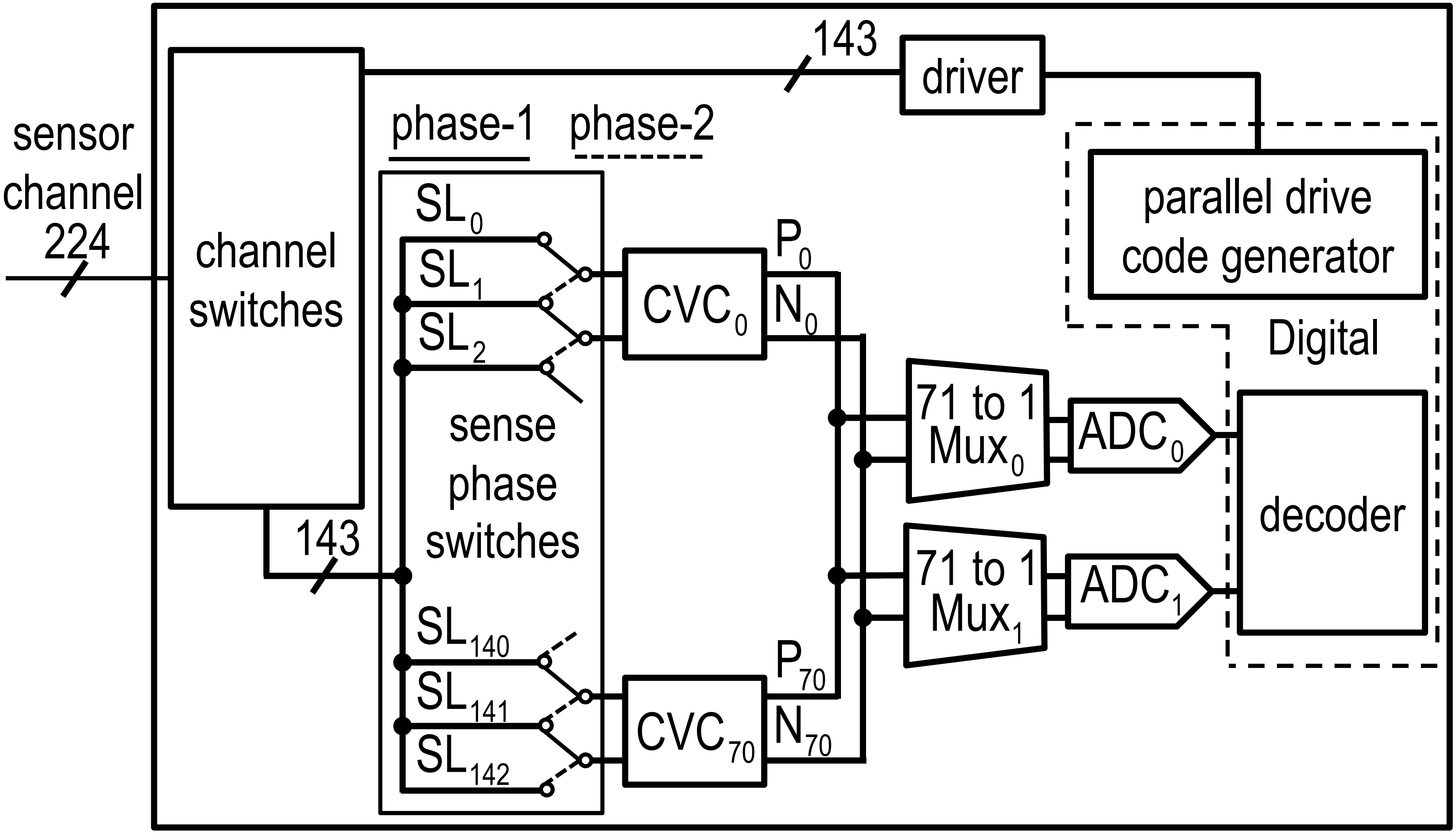
$$(2)\quad \mathbf{Voutp} - \mathbf{Voutm} \propto \boxed{\frac{(\Delta\mathbf{C}_{j(k+1)} - \Delta\mathbf{C}_{jk})\bullet \mathbf{Vd}}{\mathbf{Cci}}}$$

Single-ended

Differential

*Vd : driving voltage , Vnoise : noise voltage

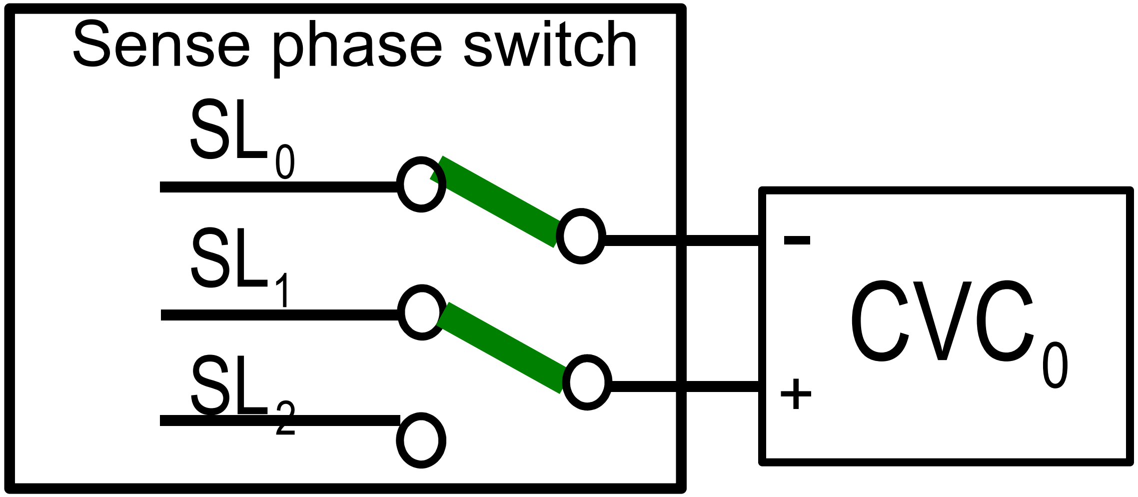
AFE block diagram



CVC: charge-to-voltage converter
ADC: analog-to-digital converter
Mux: multiplexer
SL : sense line

Sense phase switch operation

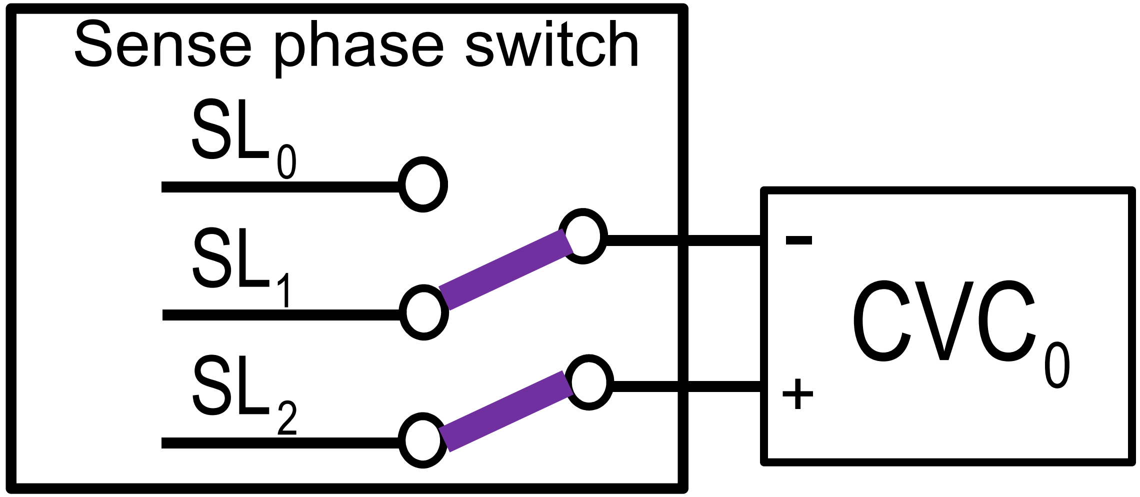
Phase-1



CVC No.	phase-1	phase-2
CVC_0	$SL_1 - SL_0$	$SL_2 - SL_1$
CVC_1	$SL_3 - SL_2$	$SL_4 - SL_3$
…	…	…
CVC_p	$SL_{2p+1} - SL_{2p}$	$SL_{2p+2} - SL_{2p+1}$
…	…	…
CVC_{70}	$SL_{141} - SL_{140}$	$SL_{142} - SL_{141}$

Sense phase switch operation

Phase-2



CVC No.	phase-1	phase-2
CVC_0	$SL_1 - SL_0$	$SL_2 - SL_1$
CVC_1	$SL_3 - SL_2$	$SL_4 - SL_3$
…	…	…
CVC_p	$SL_{2p+1} - SL_{2p}$	$SL_{2p+2} - SL_{2p+1}$
…	…	…
CVC_{70}	$SL_{141} - SL_{140}$	$SL_{142} - SL_{141}$

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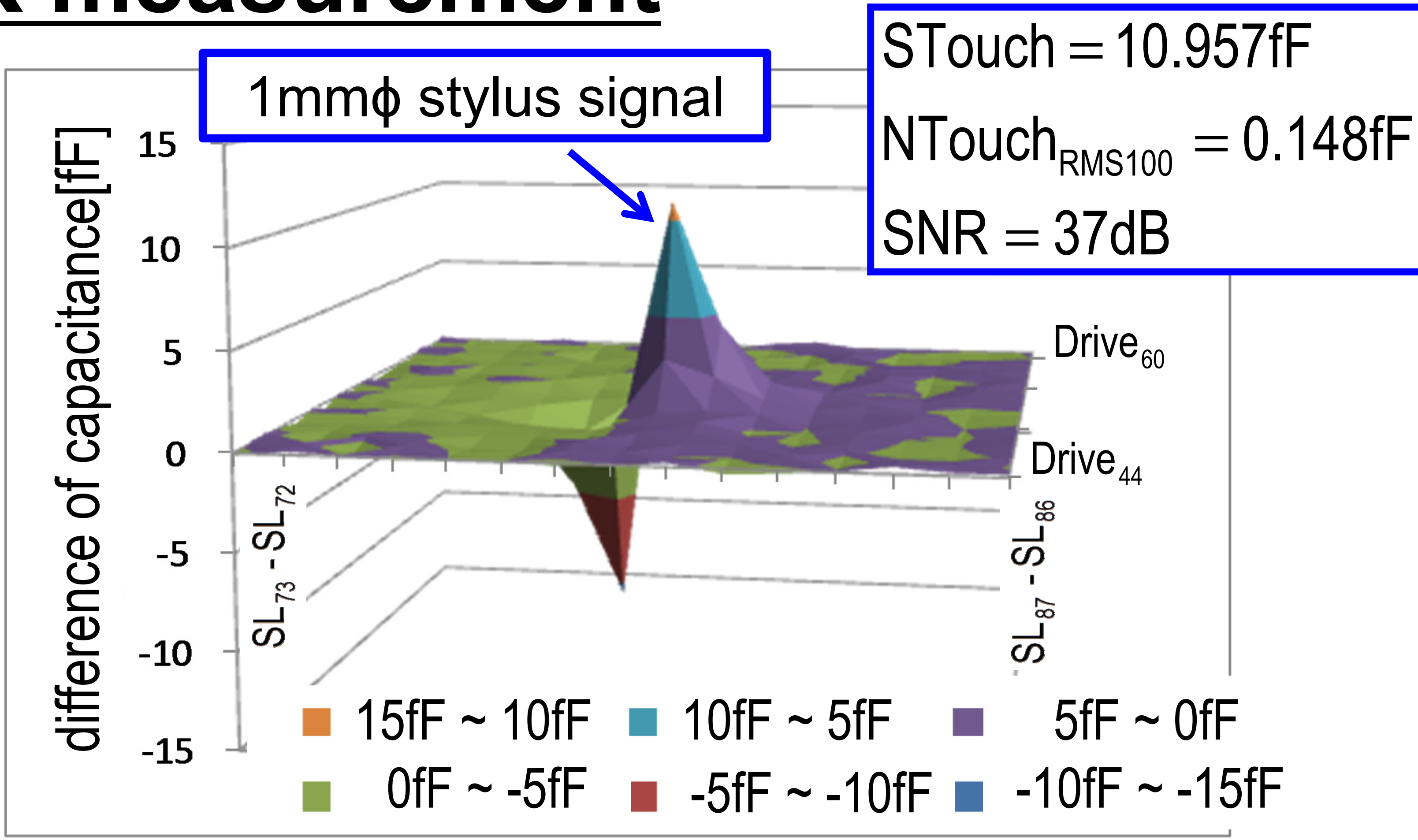
SNR measurement



$$\mathbf{STouch} = \mathbf{Signal}_{\mathbf{Touch,\,AVG100}} - \mathbf{Signal}_{\mathbf{Untouch,\,AVG100}}$$

$$\mathbf{SNR(dB)} = \mathbf{20log}\frac{\mathbf{STouch}}{\mathbf{NTouch}_{\mathbf{RMS100}}}$$

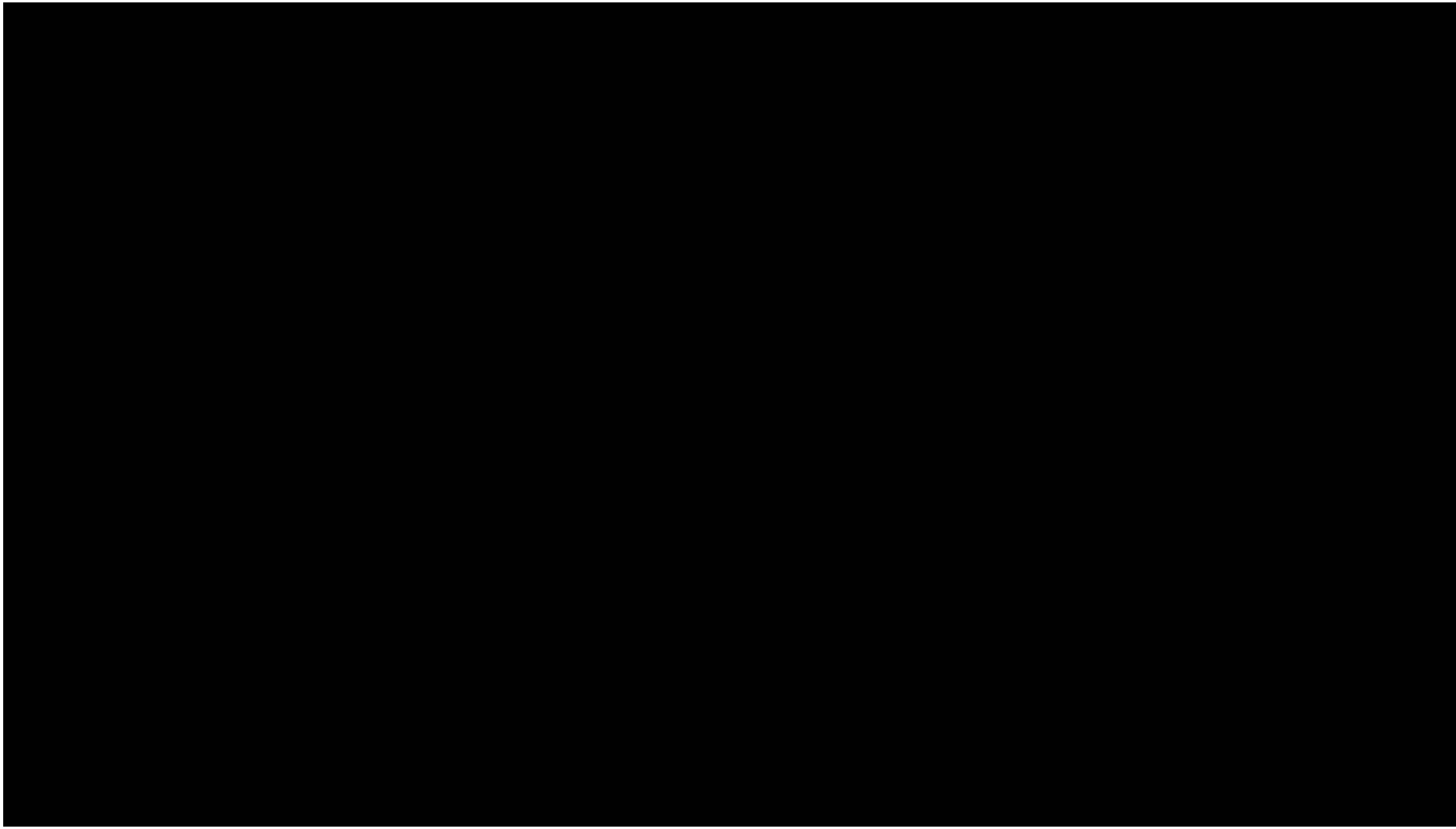
$$\mathbf{NTouch}_{\mathbf{RMS100}} = \sqrt{\frac{\sum_{n=0}^{n=99}\left(\mathbf{Signal}[n] - \mathbf{Signal}_{\mathbf{Touch}}\right)^2}{\mathbf{100}}}$$

Performance Summary

		[3]	[4]	This work			
Size[inch]		10.1	5	**32**		**70**	
Number of channels (Drive × Sense)		27ch × 43ch	30ch × 24ch	**78ch × 138ch**		**140ch × 248ch**	
Mode		Undescribed	High SNR (CDMS DS-SC)	Slow	Normal	Slow	Normal
Reporting rate[Hz]		120	240	120	240	120	240
SNR[dB]	Finger	39	55	50.8	**56.6**	47.5	52.2
	Stylus (1mmΦ)	Undescribed	35	31.6	**37.4**	31.5	**37.7**
Power consumption	Total[mW]	18.7	52.8	214.7	559.9	562.8	1247.0
	Per node [uW/node]	16.1	73.3	19.9	52.0	**16.2**	35.9

[3] J.-H. Yang, ISSCC 2013 [4] H. Shin, ISSCC2013

Demonstration video



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Summary

1. An Analog Front-End IC for a mutual-capacitance touch-sensing is developed.

- large number of channels : 143×81
- fast reporting rate : 240Hz
- high SNR

  over 37dB @ 1mm diameter stylus

  over 52dB @ 9mm diameter artificial finger

  - Verified with a 32-inch and a 70-inch metal mesh sensor on LCD.

2. Key techniques

- Parallel drive
- Fully differential sensing scheme

Thank you for your attention.

A 1mm-Pitch 80x80-Channel 322Hz-Frame-Rate Touch Sensor with Two-Step Dual-Mode Capacitance Scan

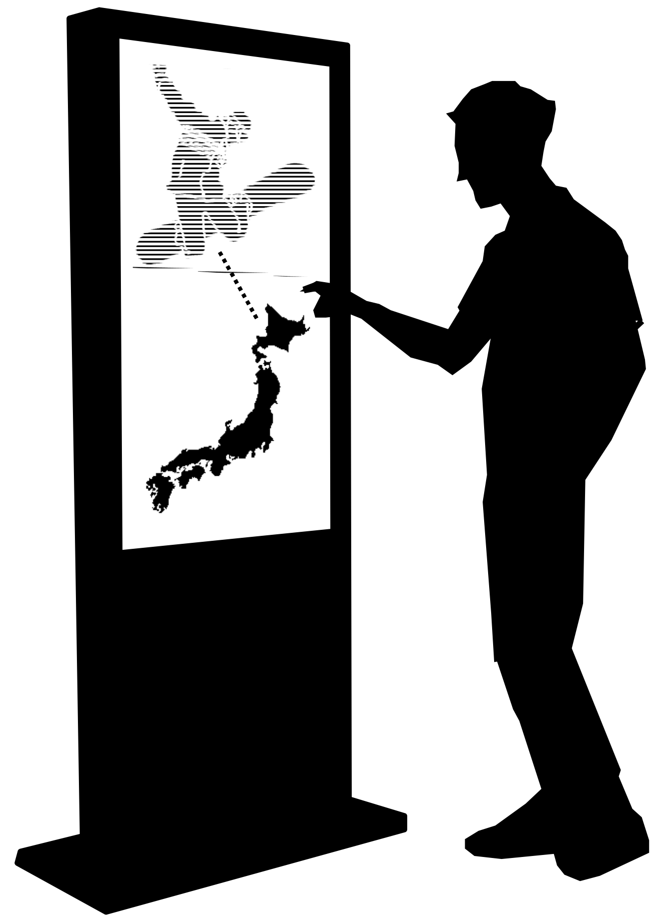
Noriyuki Miura[1], *S. Dosho*[2], *S. Takaya*[1], *D. Fujimoto*[1], *T. Kiriyama*[1], *H. Tezuka*[2], *T. Miki*[2], *H. Yanagawa*[2], *and M. Nagata*[1]

[1]*Kobe University*, [2]*Panasonic Corporation*

Introduction

- ►**High-resolution** and **large-area** touch sensor for natural and interactive human interfaces

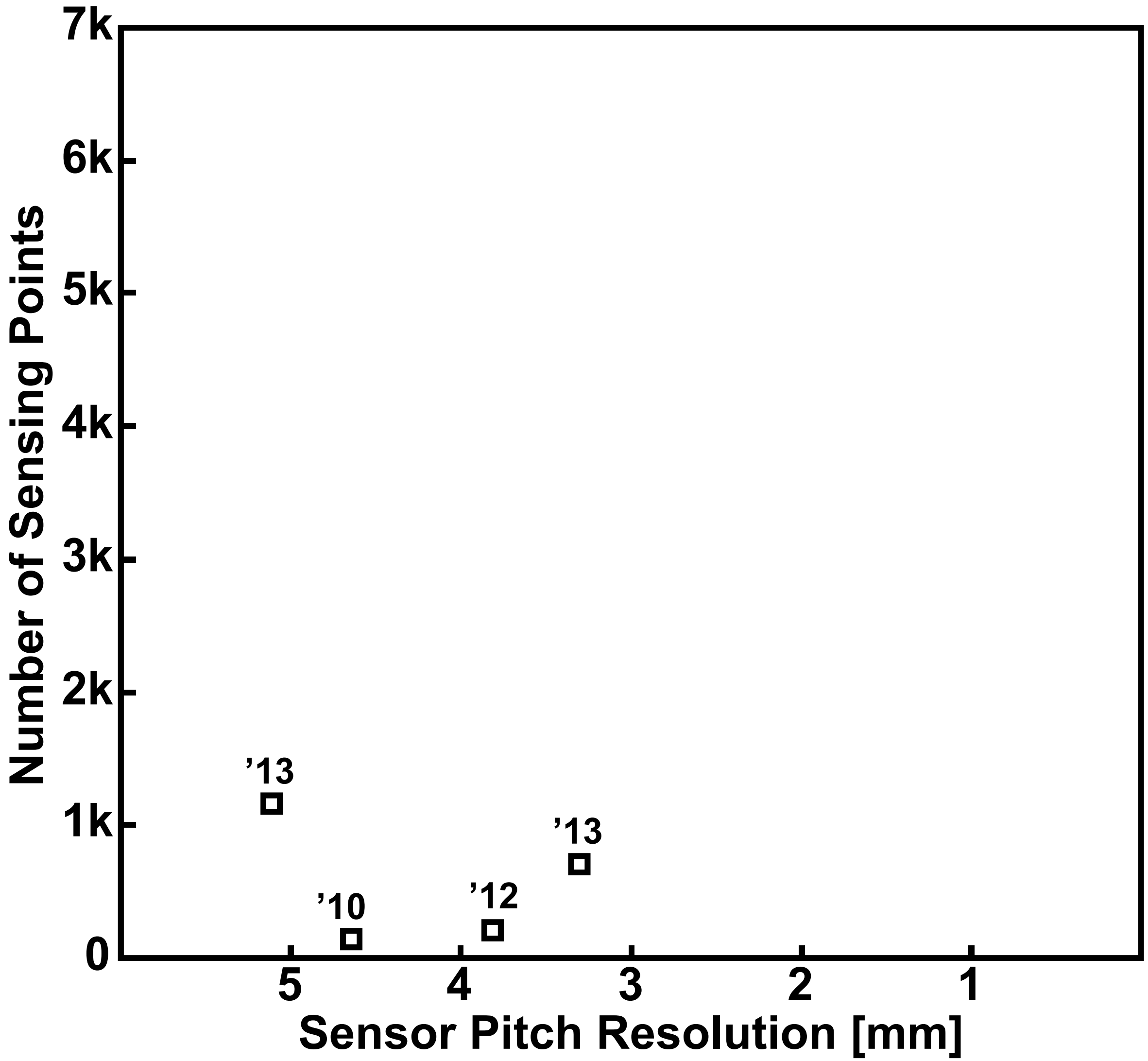
Art & Education
(Electronic Whiteboard)



Advertisement & Entertainment
(Interactive Digital Signage)

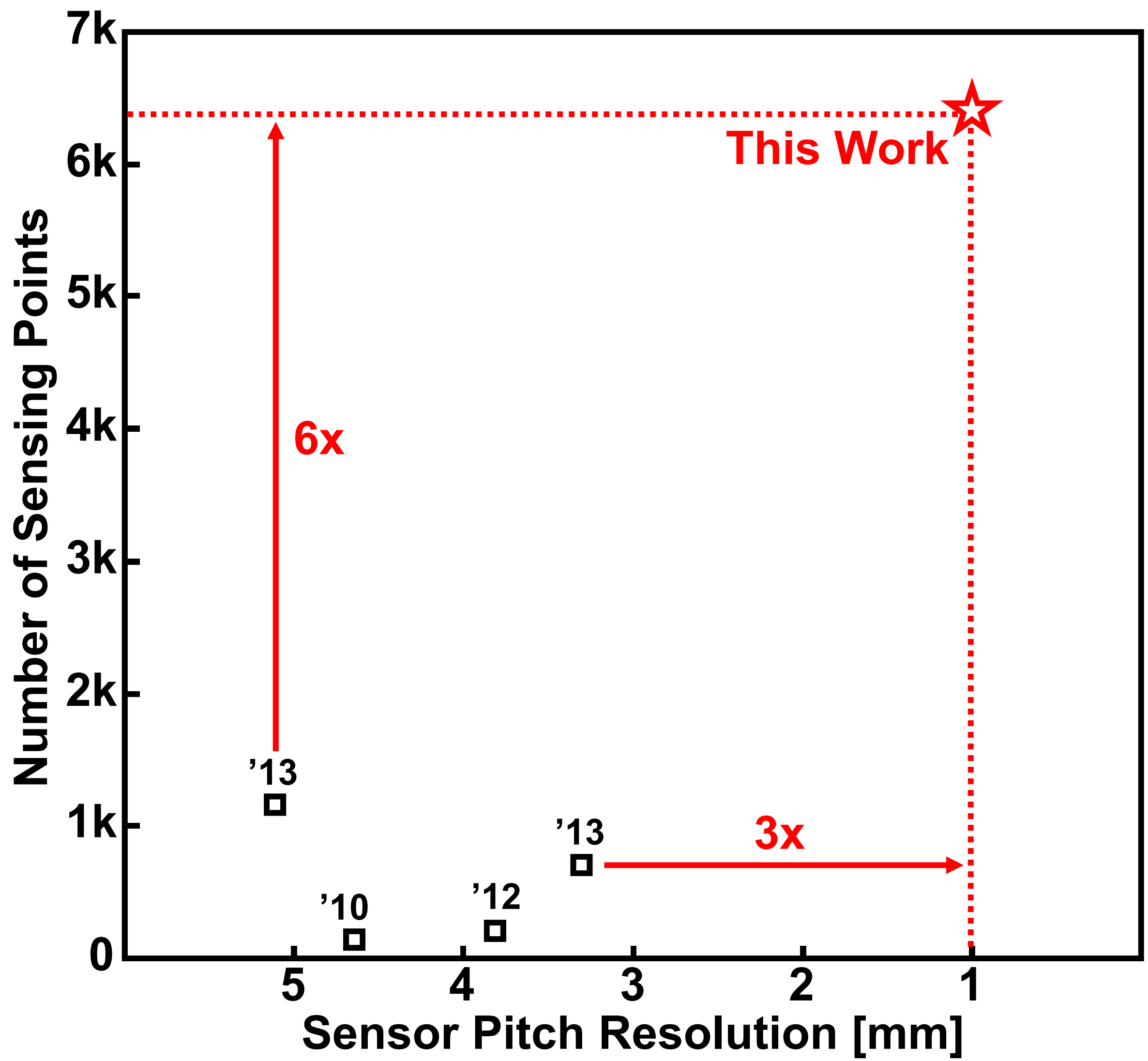
Previous Works at ISSCC

►Limited pitch resolution and sensor channels



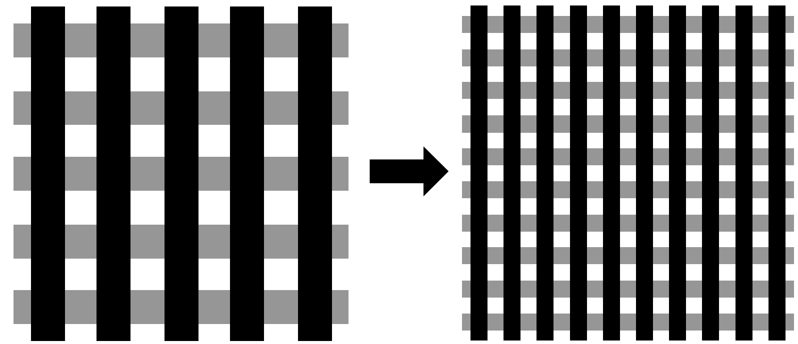
This Work

► 3x pitch resolution and 6x sensing points



Technical Challenges

- ► ① Slow frame scan rate
  - – Increased sensing points
- ► ② SNR degradation
  - – Limited electrode size



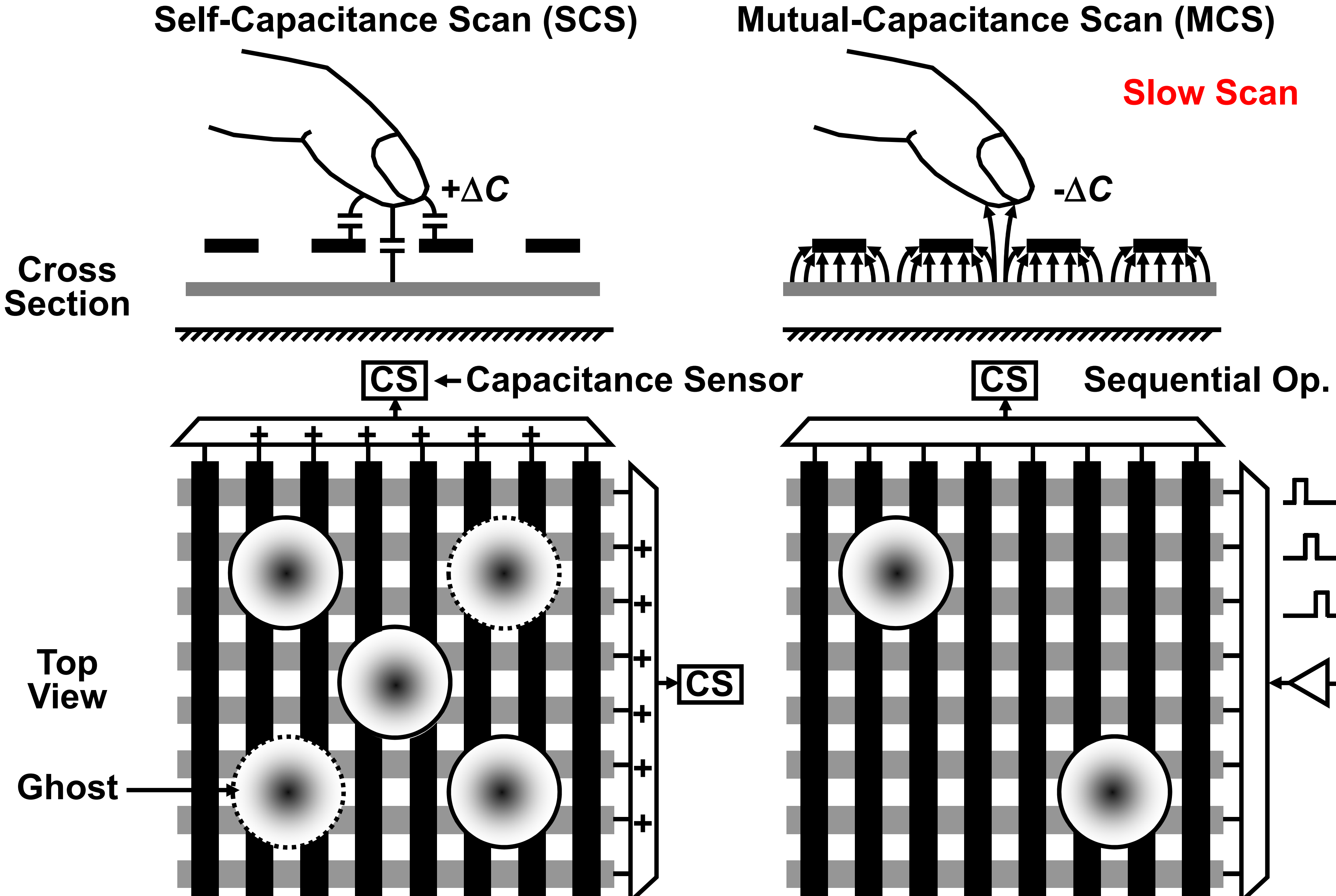
Our Solutions

- ► ① Two-step dual-mode capacitance scan
  - – Increase frame scan rate by <u>1.5x</u> for <u>6x</u> scan points
- ► ② Noise canceling/filtering in AFE circuits
  - – Keep SNR at <u>41dB</u> even with <u>1/10</u> electrode size
- ► Effective also to large-area touch sensors
  - – Same challenges in large area w/ const. resolution

Outline

- ►Introduction
- ►Two-Step Dual-Mode Capacitance Scan
  - – High Frame Scan Rate Operation
- ►Noise Reduction Techniques in AFE
  - – Keep SNR for Precise Touch Detection
- ►Test Chip Measurement
- ►Conclusion

Conventional Scan Schemes

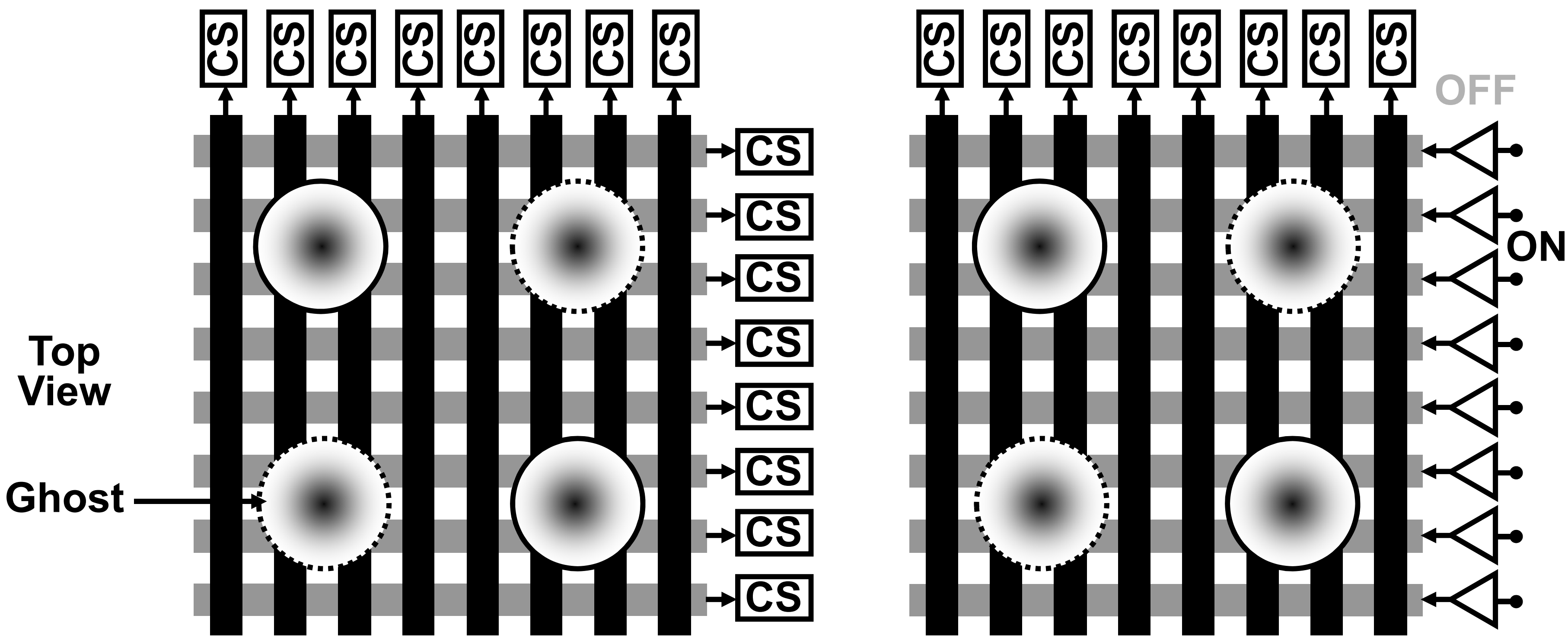


Proposed Scan Scheme

► **Two-Step Dual-Mode Capacitance Scan**

Step1: Flash SCS
"Coarse Flash Search"

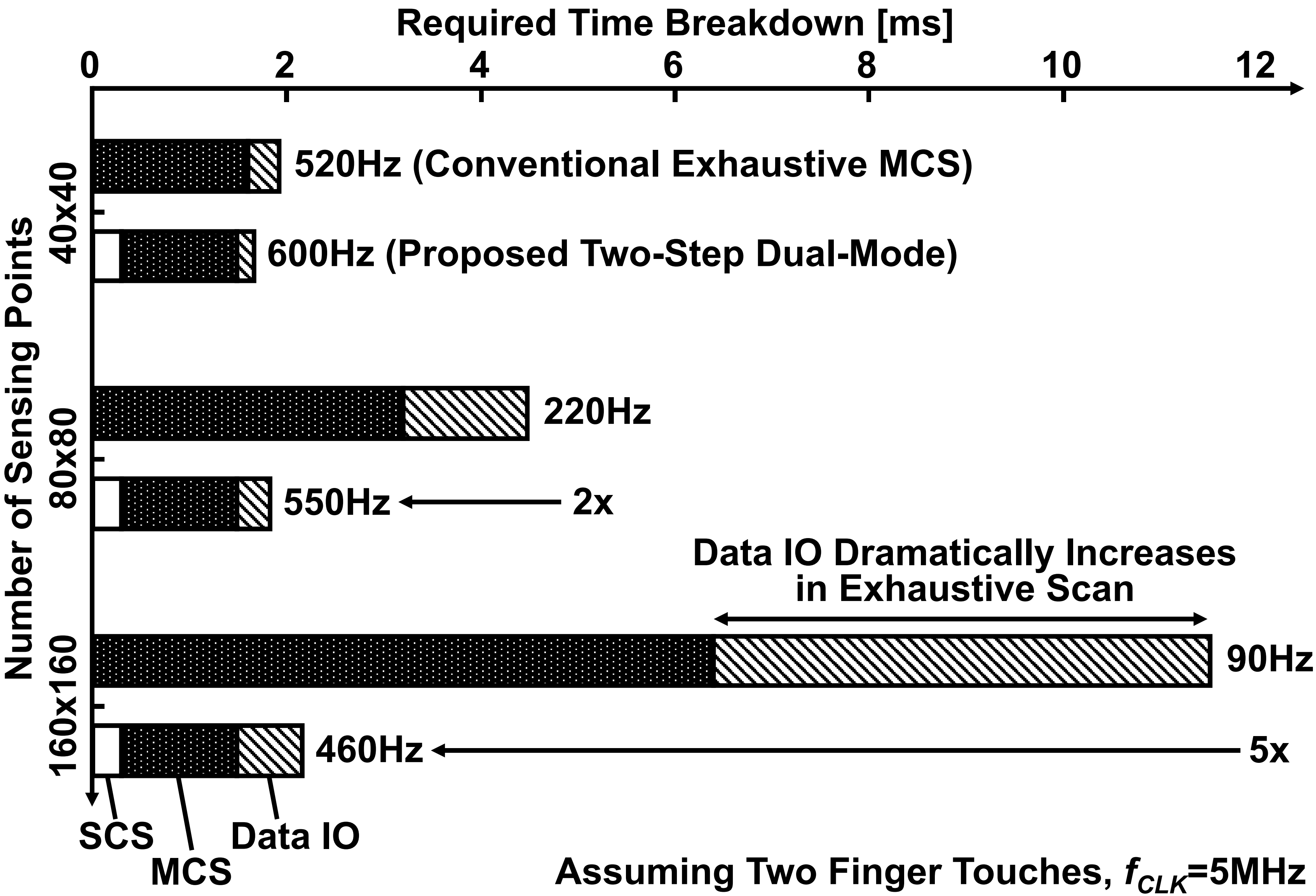
Step2: Local MCS
"Fine Selective Search"



Identifying Potential Touch Regions Including Ghost Touches

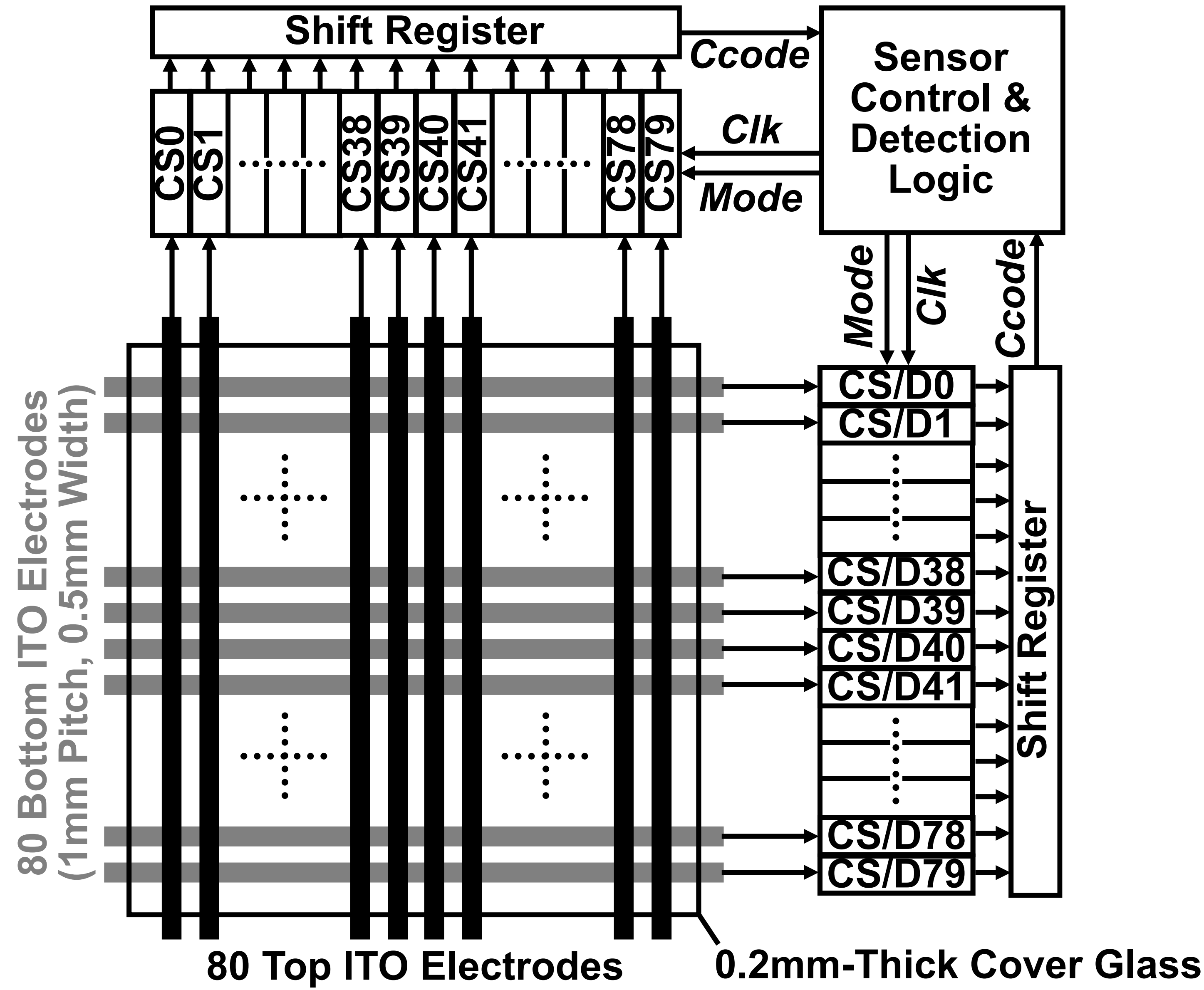
Activating Only Related Drivers & Sensors

Frame Scan Rate Calculation



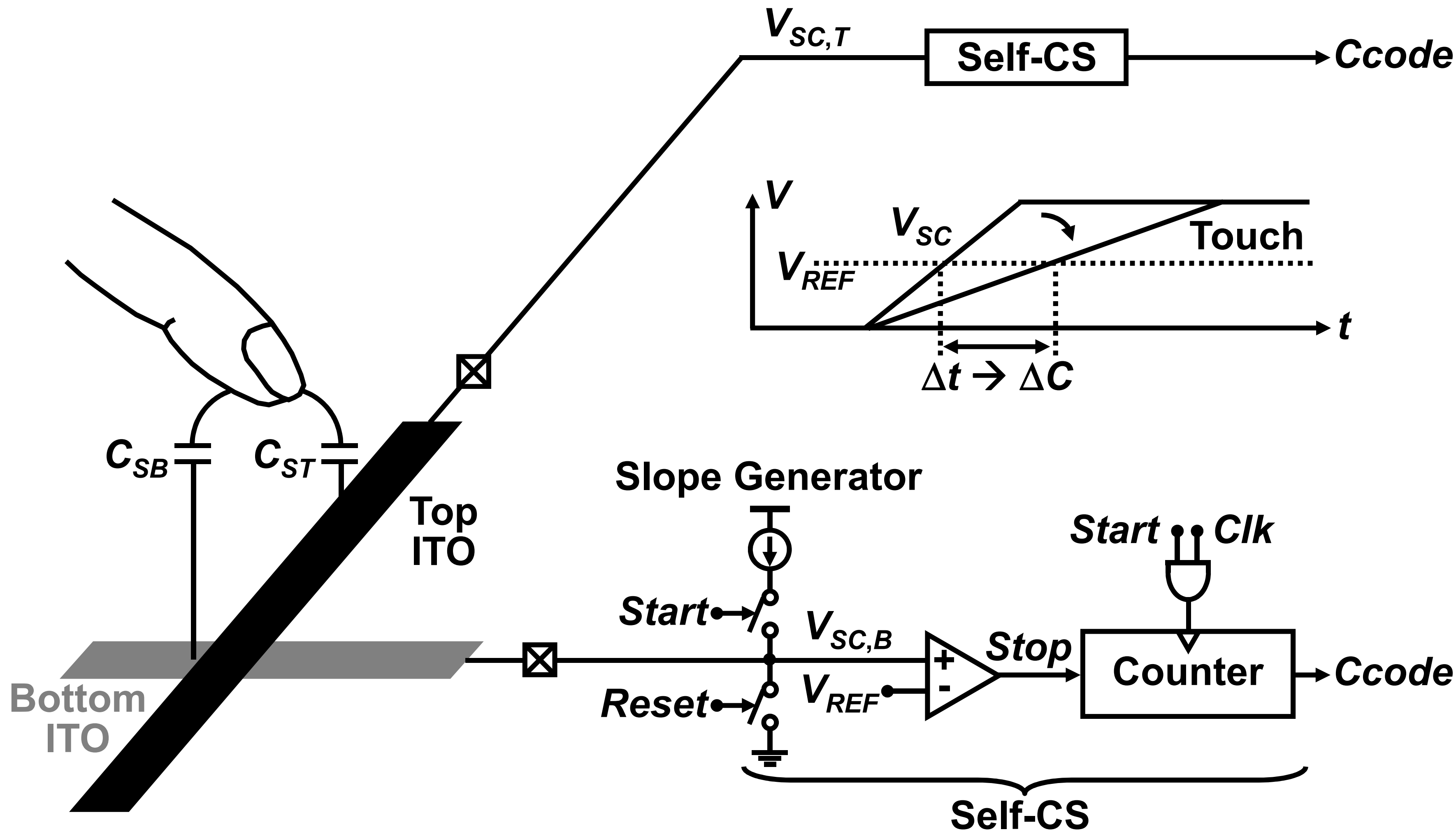
Assuming Two Finger Touches, f_{CLK}=5MHz

Sensor Architecture



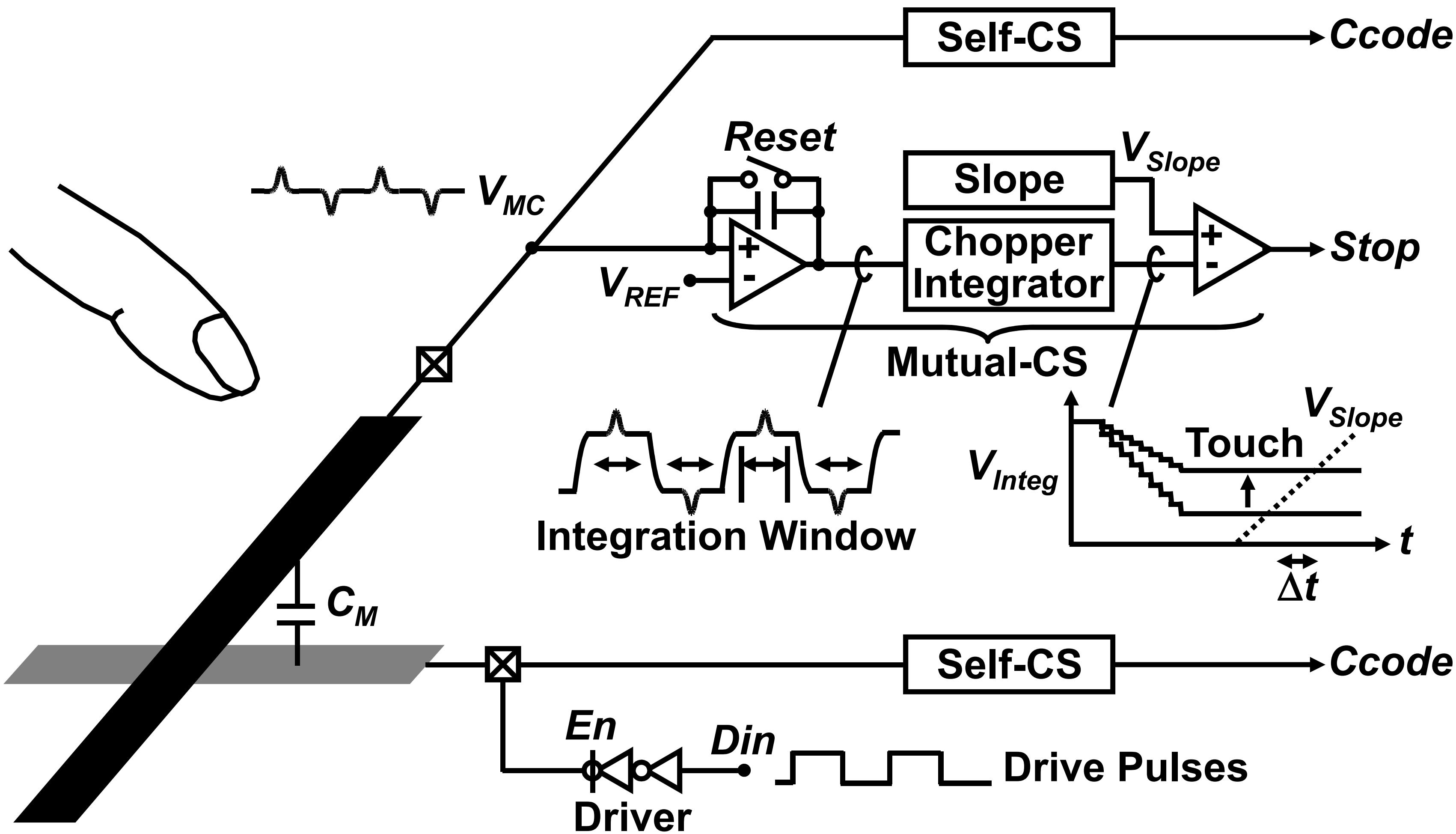
Self-Capacitance Sensor

► **Low-power time-domain slope AD convertor**



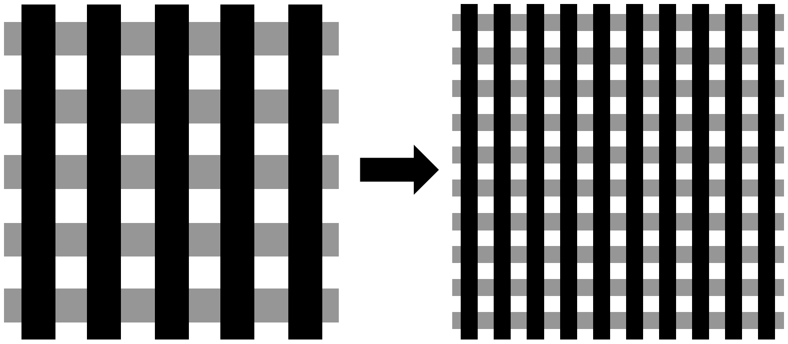
Mutual-Capacitance Sensor

► Chopper integrator and *t*-domain slope ADC



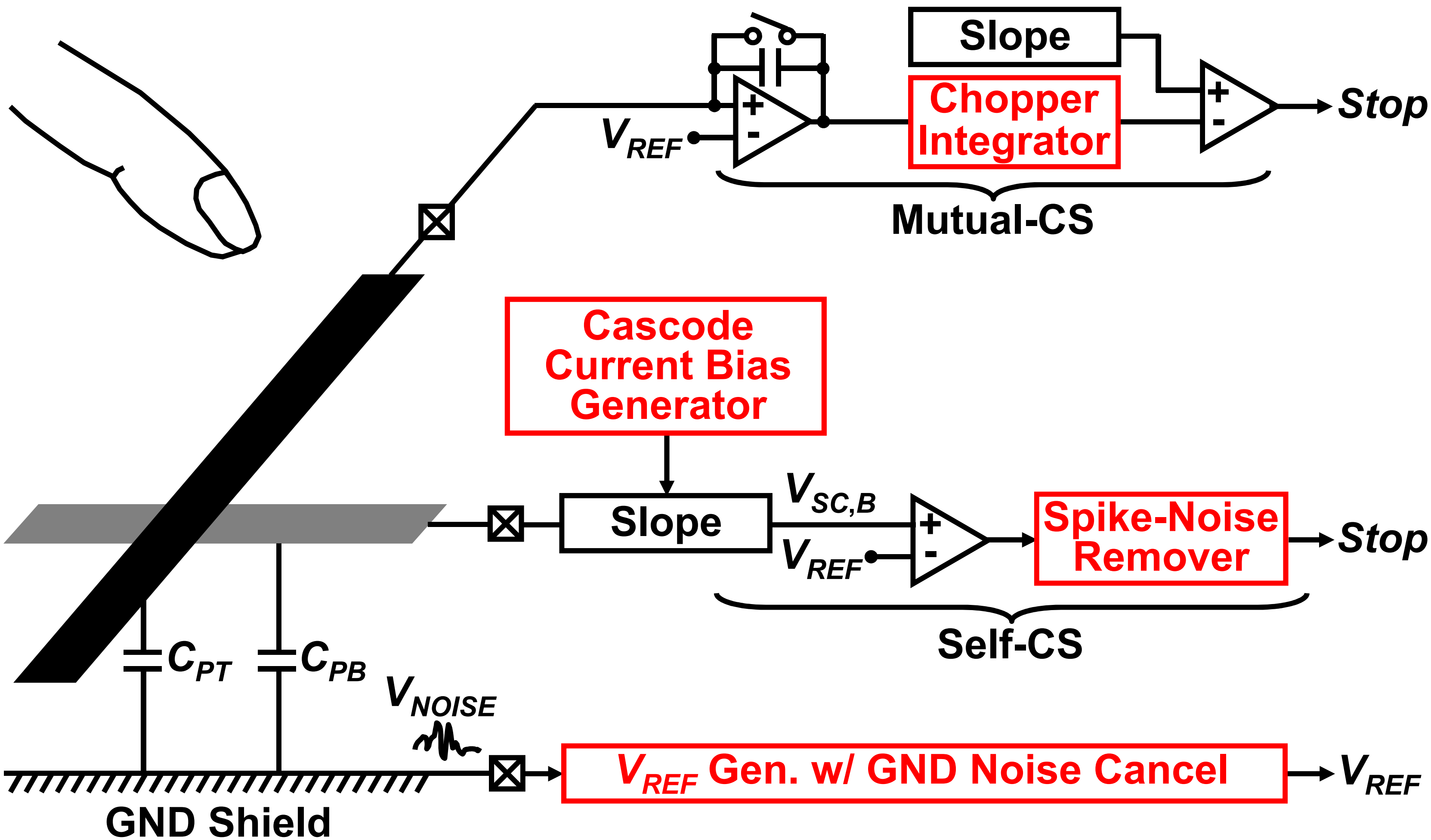
Outline

- ►Introduction
- ►Two-Step Dual-Mode Capacitance Scan
- ►**Noise Reduction Techniques in AFE**
  - – **Keep SNR for Precise Touch Detection even with Small Electrode in High Resolution**
- ►Test Chip Measurement
- ►Conclusion



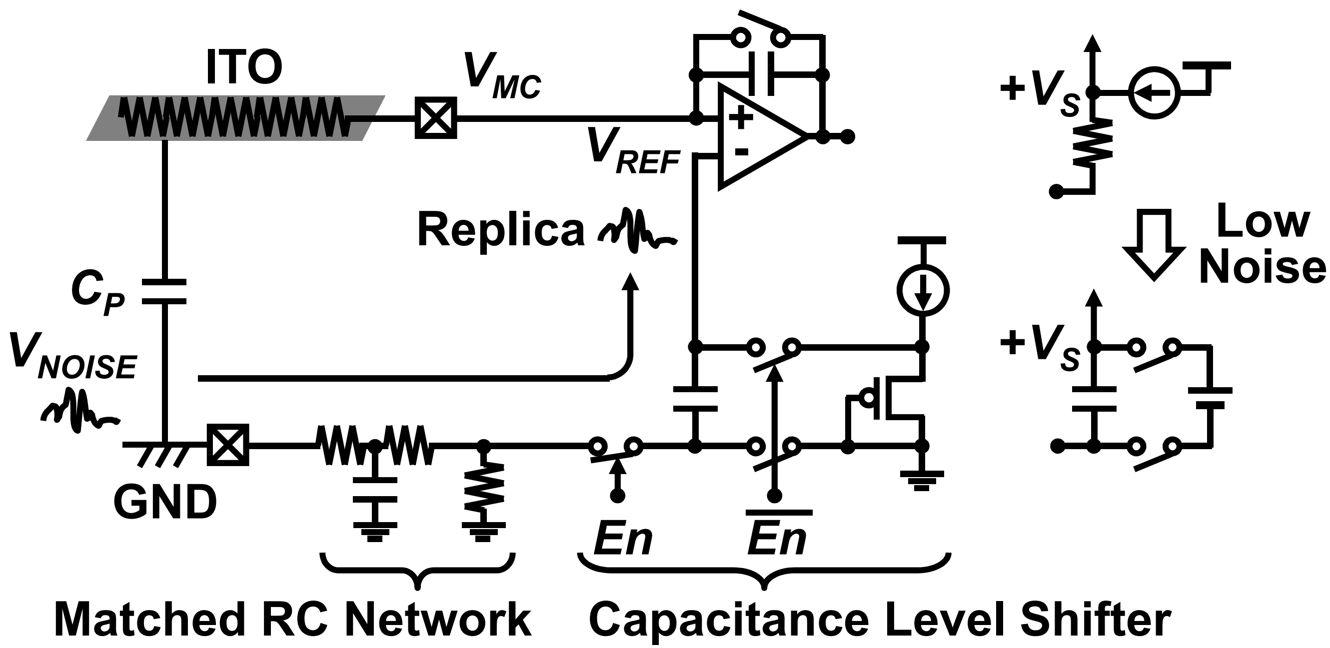
Noise Reduction Overview

- ►Thorough noise reduction techniques applied



V_{REF} Gen. w/ GND Noise Cancel

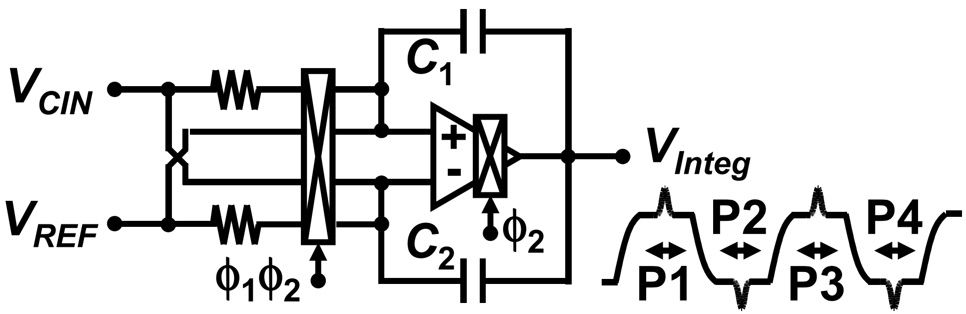
►Replica cancel by CM rejection at opamp

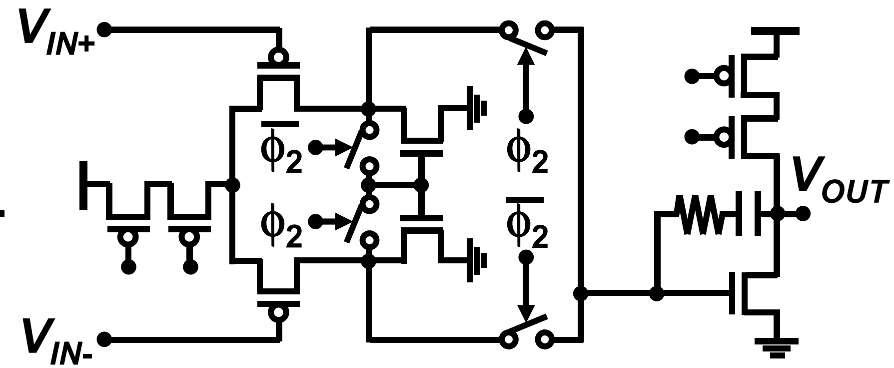


- Simulated noise in mutual-CS <8mV @ C_P=40pF
- Support C_P<80pF (equivalent to <u>60cm</u> ITO)

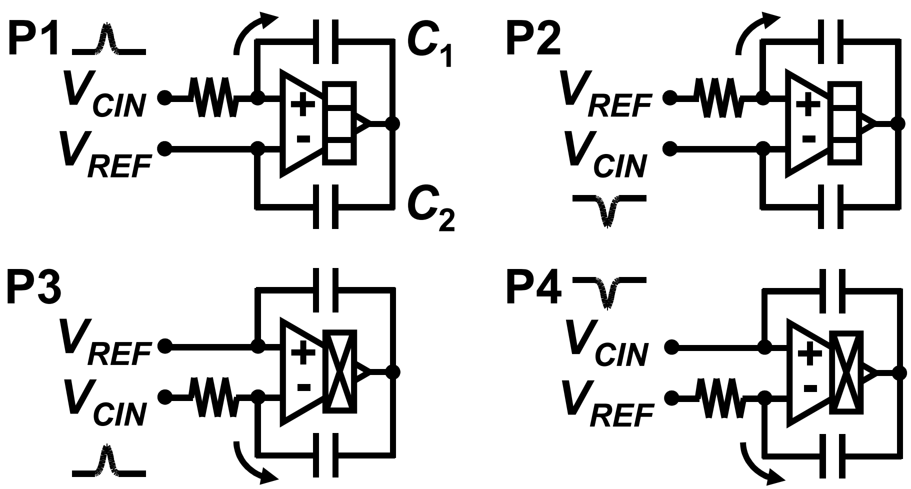
4-Phase Chopper Integrator

- ►Offset removal & bi-polar pulse integration





Chopper Opamp w/ Inner Switch



No Switch in C_1C_2 Feedback Path

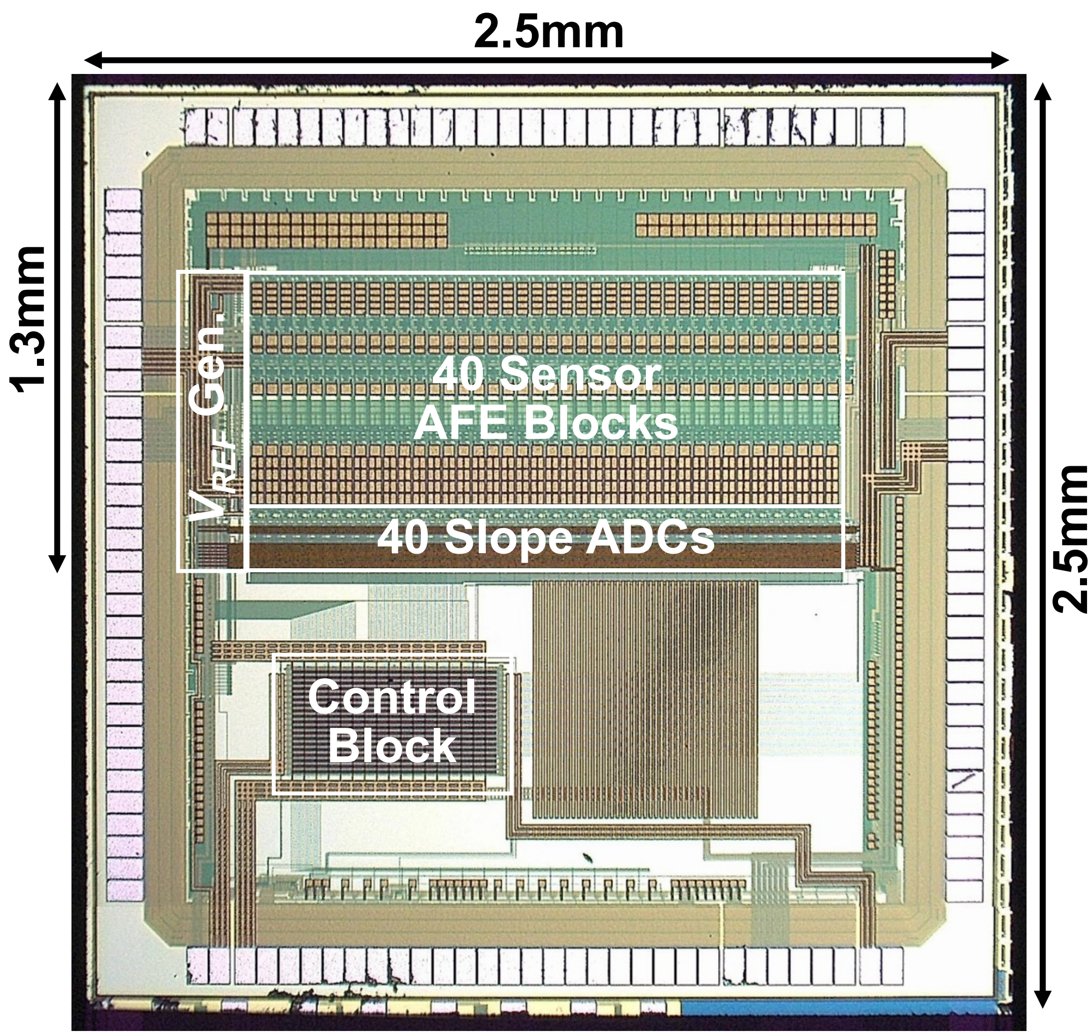
Fast Settling
Relaxed Phase Control
(Low Noise)

- – Chopper cuts low-frequency noise and offset
- – Integration cuts high-frequency noise

Outline

- ►Introduction
- ►Two-Step Dual-Mode Capacitance Scan
- ►Noise Reduction Techniques in AFE
- ►**Test Chip Measurement**
- ►Conclusion

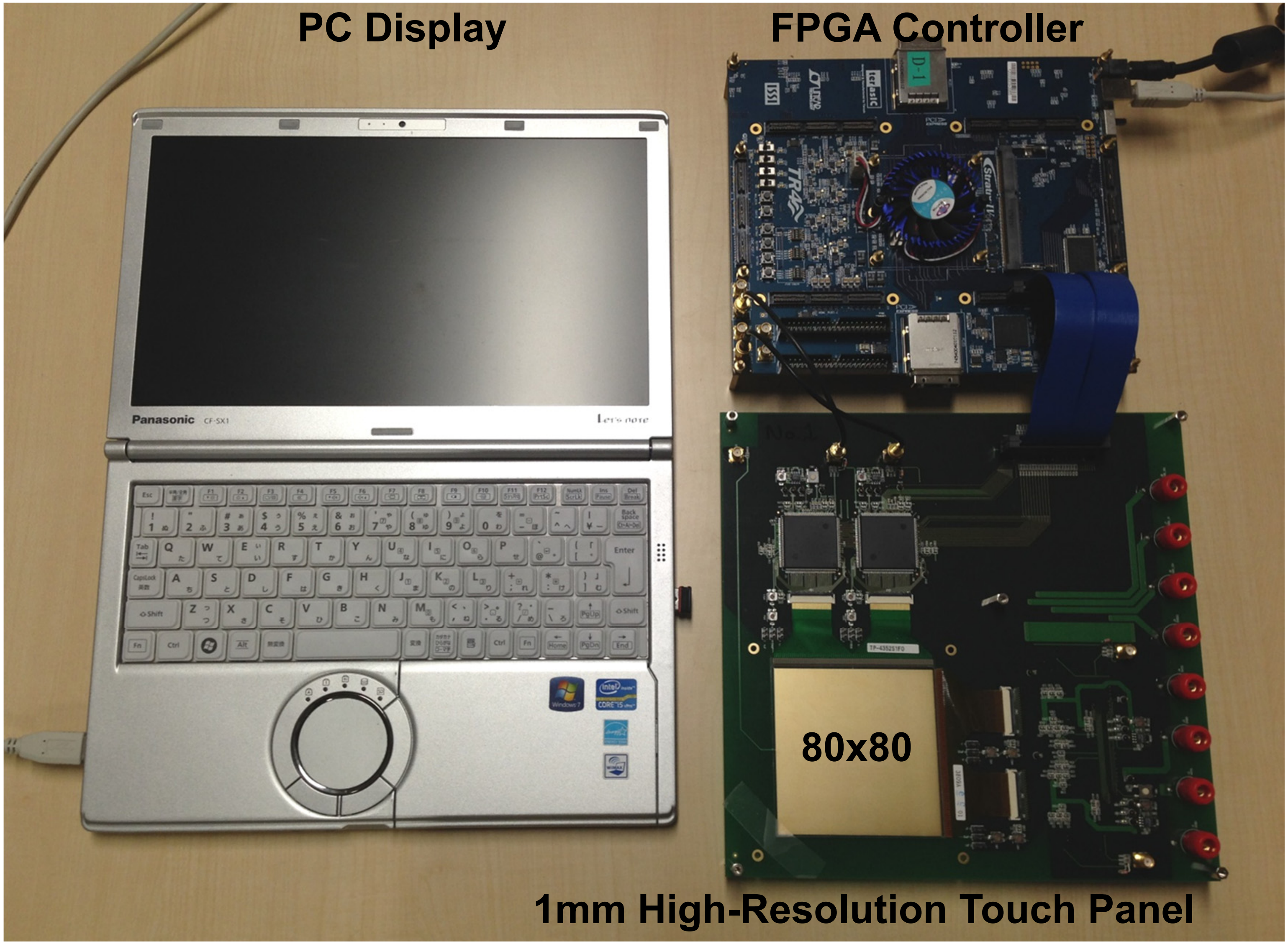
Die Photo



Fabricated in 0.35μm CMOS

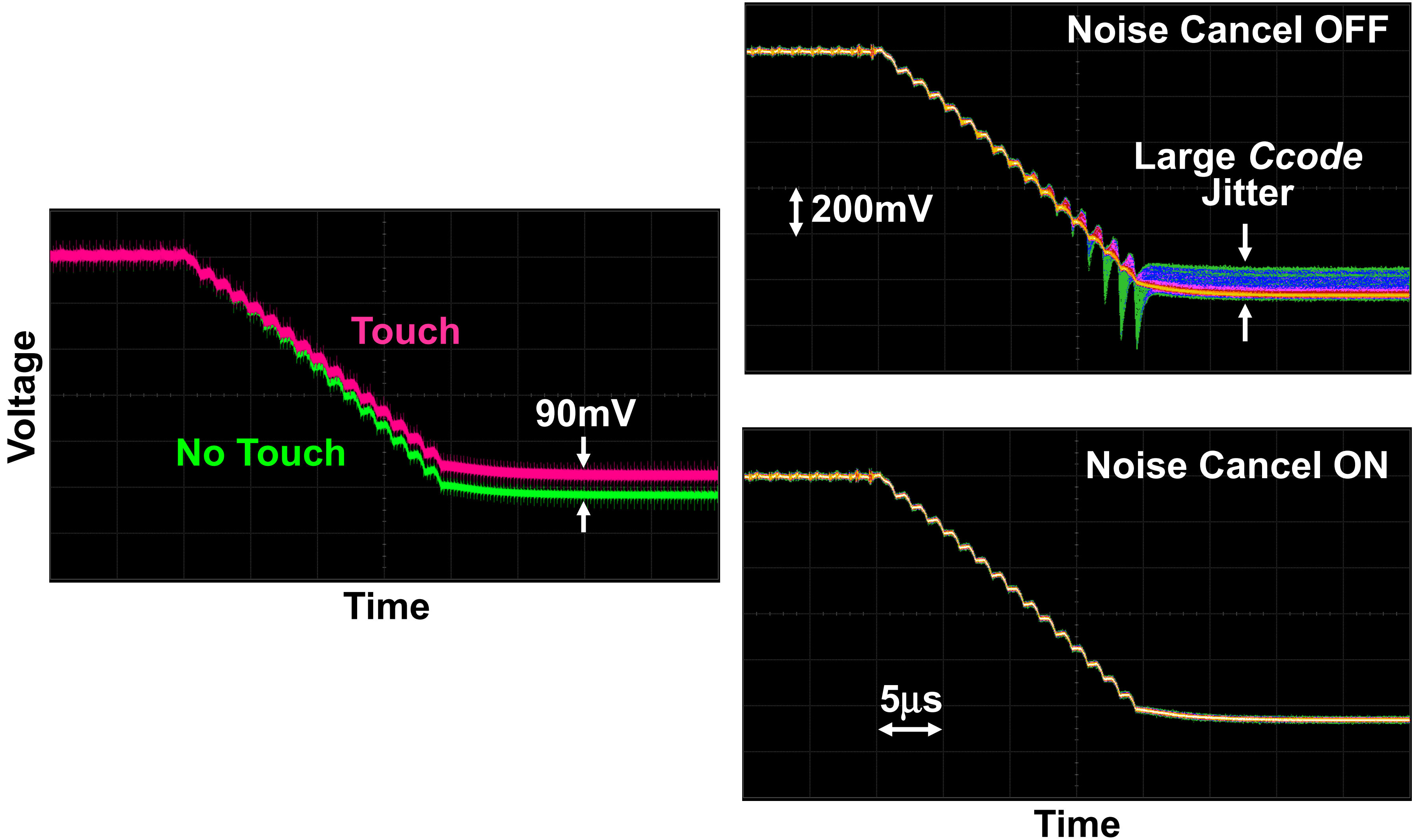
40 Sets of Self-CS, Mutual-CS, Driver Blocks Integrated
4 Chips Used to Build 80x80 Channel Touch Sensor

Measurement Setup



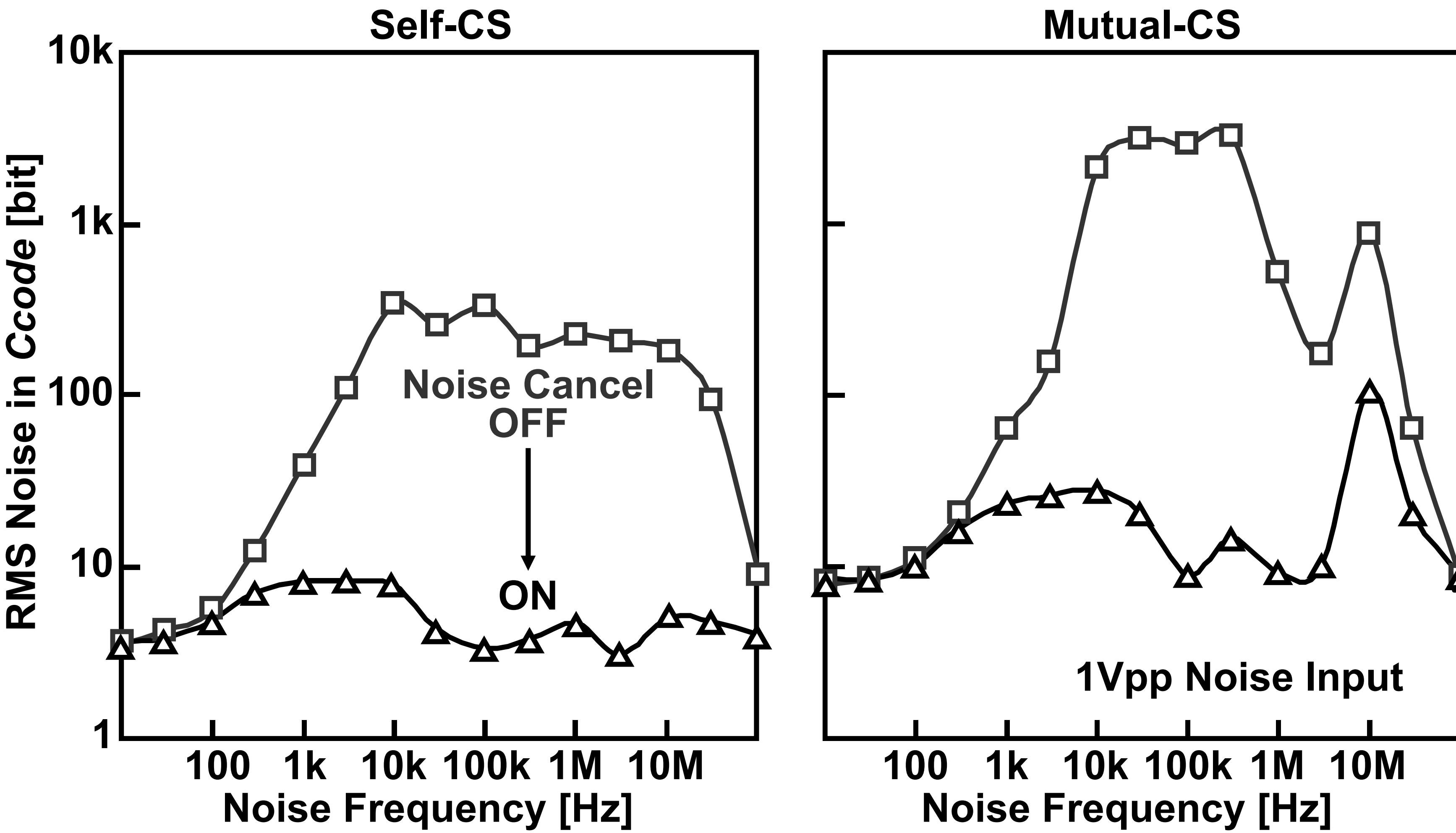
Waveform Snapshot

► **Successful touch detection by Mutual-CS**



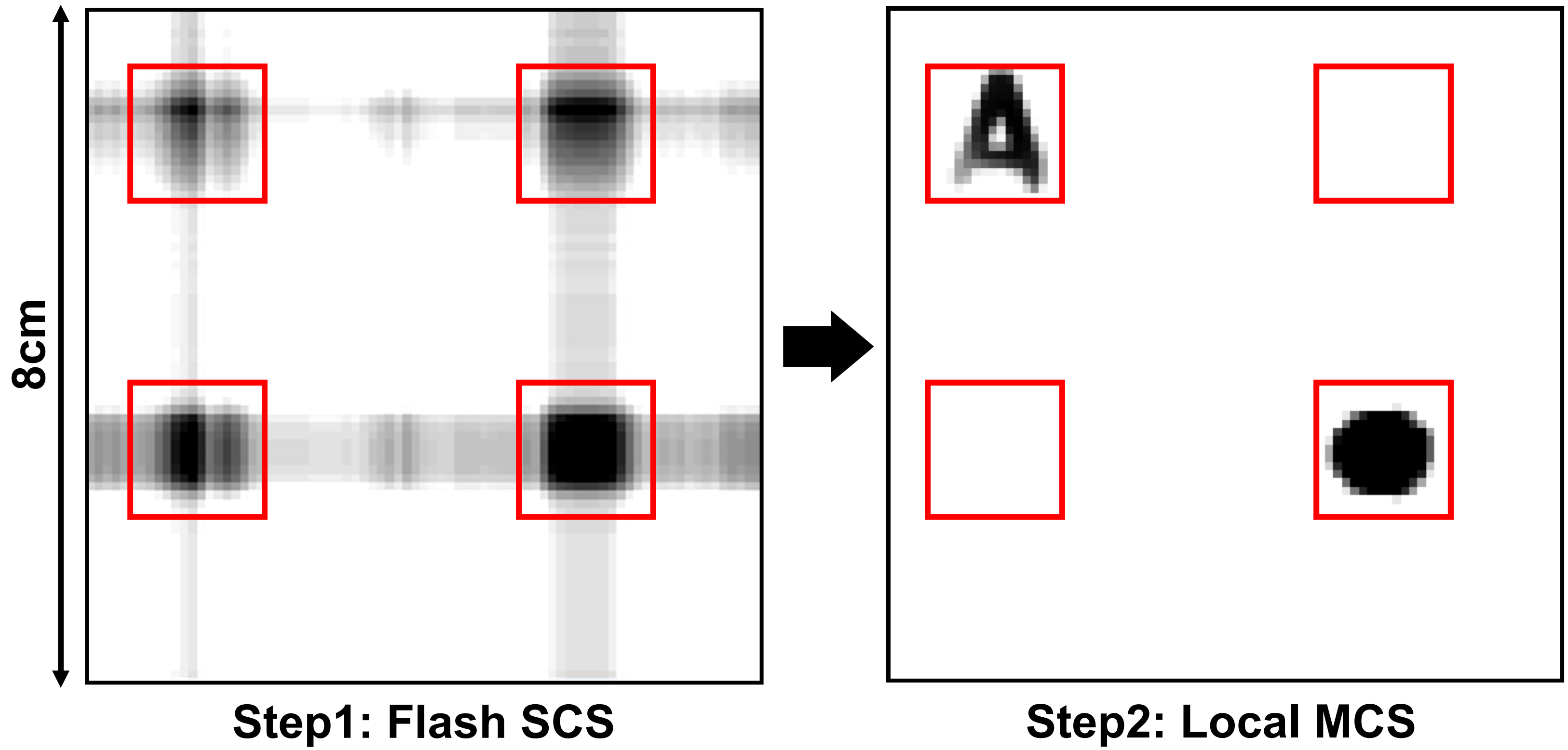
Noise Filtering

► Effective noise removal over wideband



Dual-Mode Operation

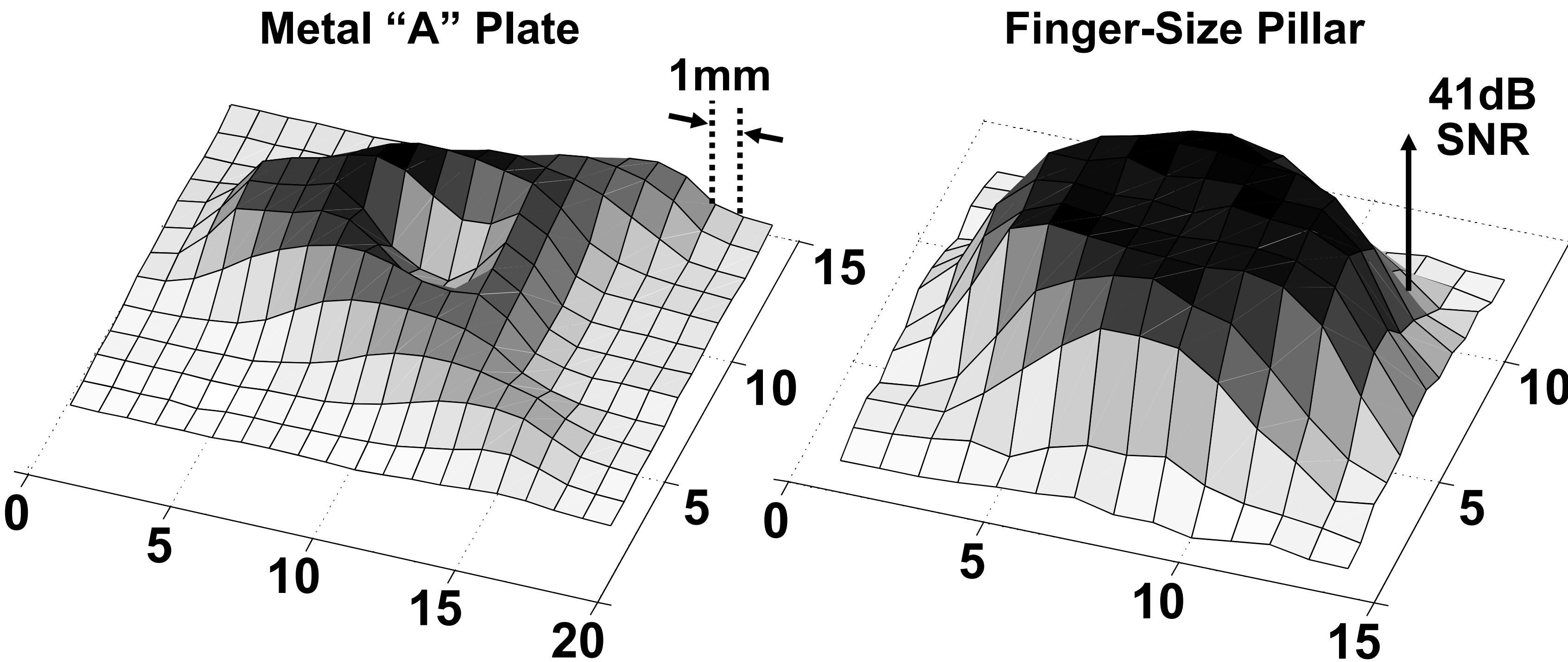
► 322Hz-frame-rate high-speed operation



Without Averaging Process

Capacitance Distribution

► 1mm-high-resolution smooth *C* distribution



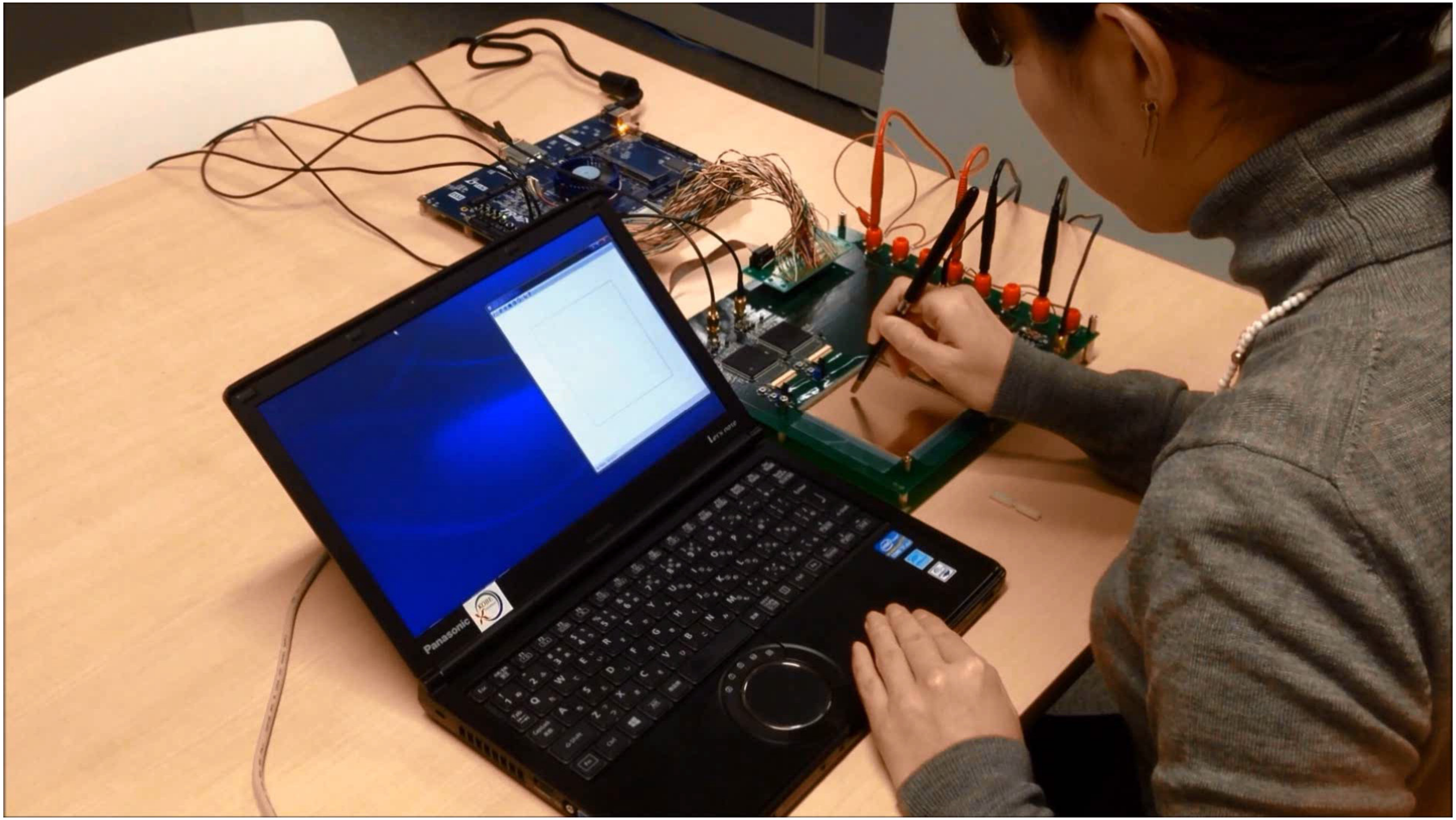
Without Averaging Process

Performance Summary

	J.-H. Yang, (ISSCC'13)	H. Shin, (ISSCC'13)	This Work
Capacitance Sensing Type	Mutual	Mutual	Self/Mutual Dual Mode
Channel Pitch	5mm	3mm	1mm (1/3)
Number of Channels	27x43	24x30	80x80 (6x)
Frame Rate Scan Points / Sec.	120Hz 0.14Mpoints	240Hz 0.17Mpoints	322Hz 2.06Mpoints (10x)
Power Consumption Energy / Channel	18.7mW 134nJ	52.8mW 306nJ	21.8mW 11nJ (1/12)
Chip Layout Area Area / Channel	$10.4mm^2$ $896\mu m^2$	$14.9mm^2$ $2069\mu m^2$	$13.7mm^2$ $214\mu m^2$ (1/4)
SNR (Finger) SNR (1mm-ϕ)	39dB	55dB 35dB	41dB 32dB
CMOS Process	$0.35\mu m$	$0.18\mu m$	$0.35\mu m$

Direct e-Brush Art Demo

Direct e-Brush Art Demo



Conclusion

►1mm-pitch 80x80ch touch sensor

– 3x finer pitch resolution + 6x multiple scan points

►Two-step dual-mode capacitance scan

– 322Hz frame scan rate even for 6x scan points

►Noise canceling/filtering circuit techniques

– 41dB high-enough SNR even with 1/10 electrode

►Demonstrated direct electrical brush art

12.5
2D Coded-Aperture-Based Ultra-Compact Capacitive Touch-Screen Controller with 40 Reconfigurable Channels

Hongjae Jang[1], Hyungcheol Shin[2], Seunghoon Ko[1], Ilhyun Yun[2] and Kywro Lee[1]

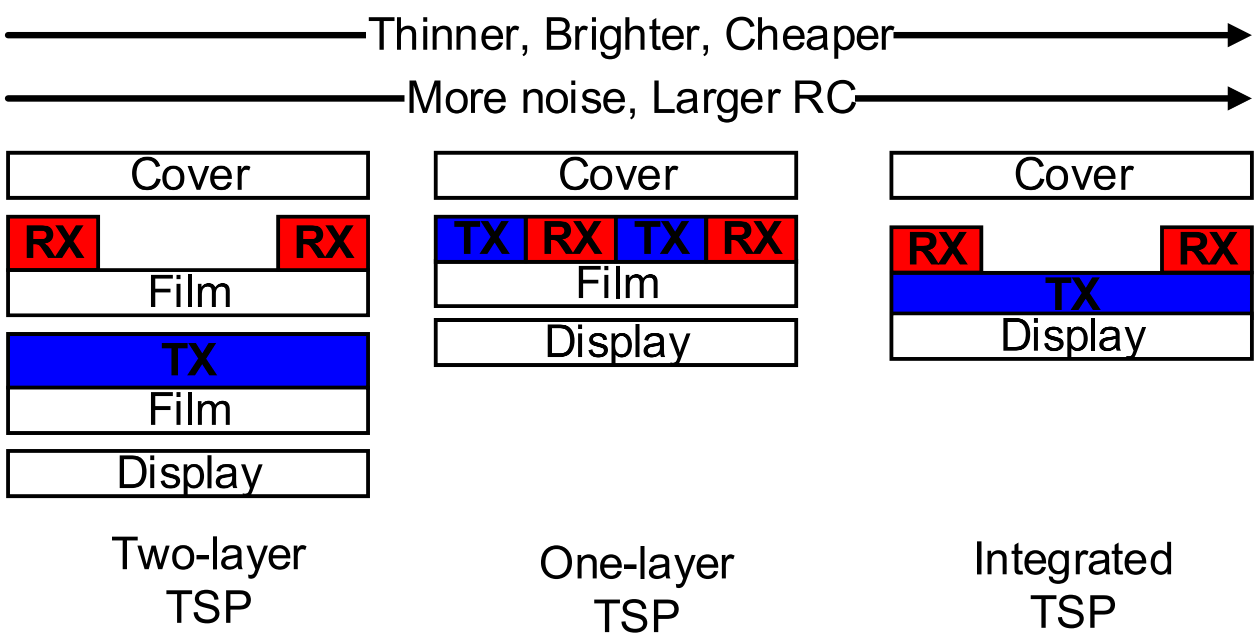
[1]KAIST, [2]Zinitix

Outline

- Introduction & Motivation
- Coded-aperture-based Read-out
- Circuit Design Details
- Experimental Results
- Summary and Conclusion

Introduction

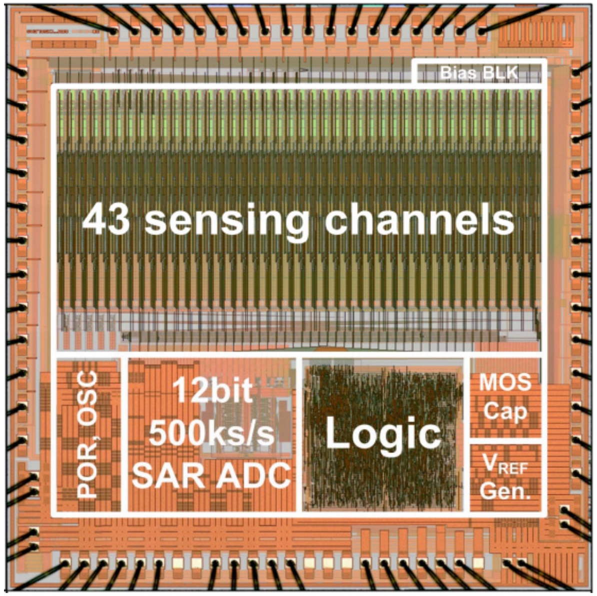
- TSPs are getting ubiquitous
- Analog read-out for mutual-cap TSP is getting tougher
  - Larger screen → More channels
  - Thinner stack-ups → More noise, Larger RC



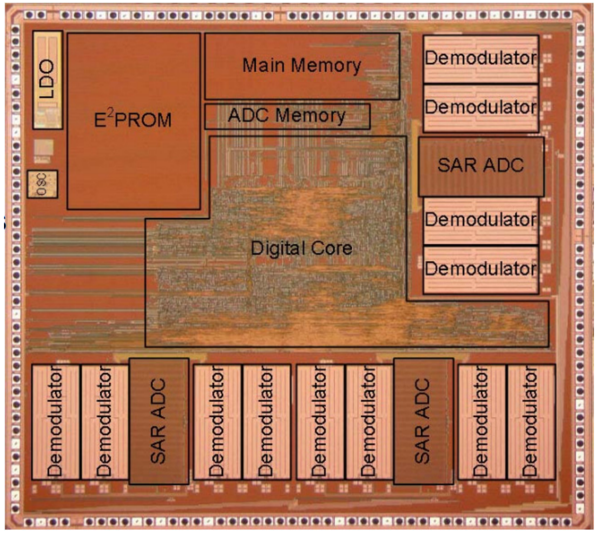
Motivation

- Column (RX) read-out circuits often need complex circuit on every parallel channels
- Easily causes analog hardware redundancies

[3]



[4]

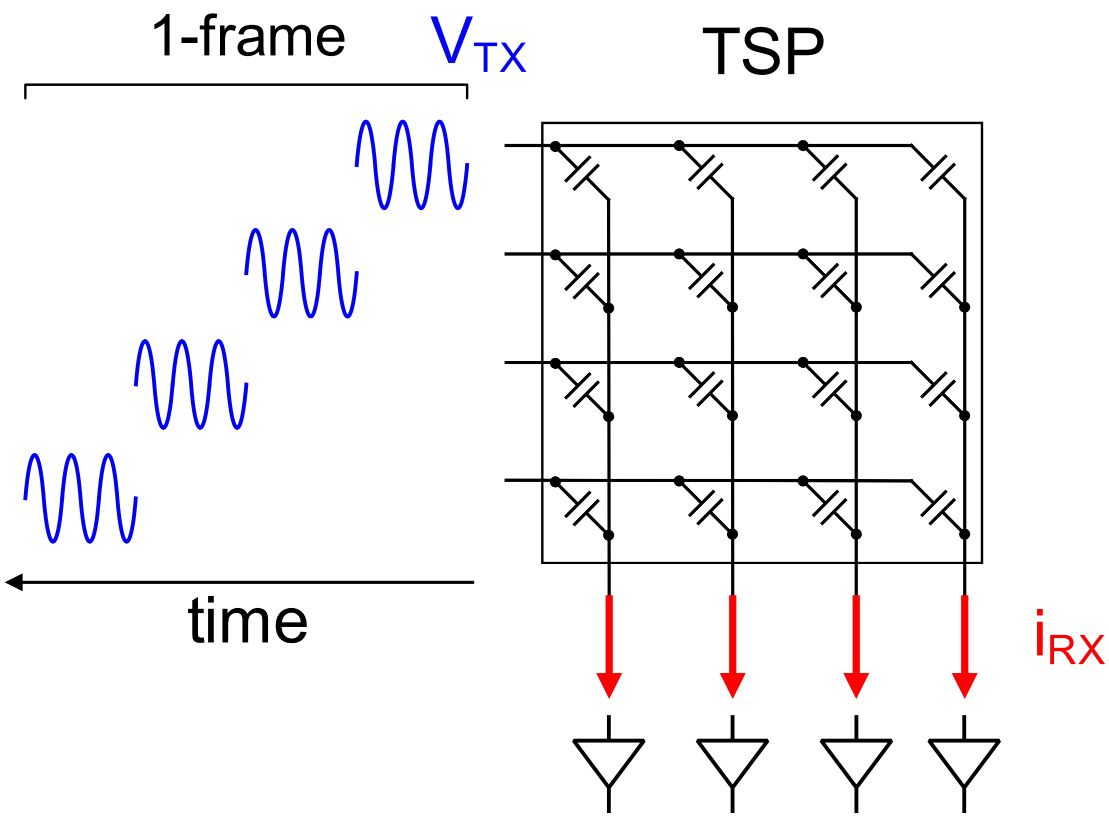


Outline

- Introduction & Motivation
- Coded-aperture-based Read-out
  - Operation
  - Architecture
- Circuit Design Details
- Experimental Results
- Summary and Conclusion

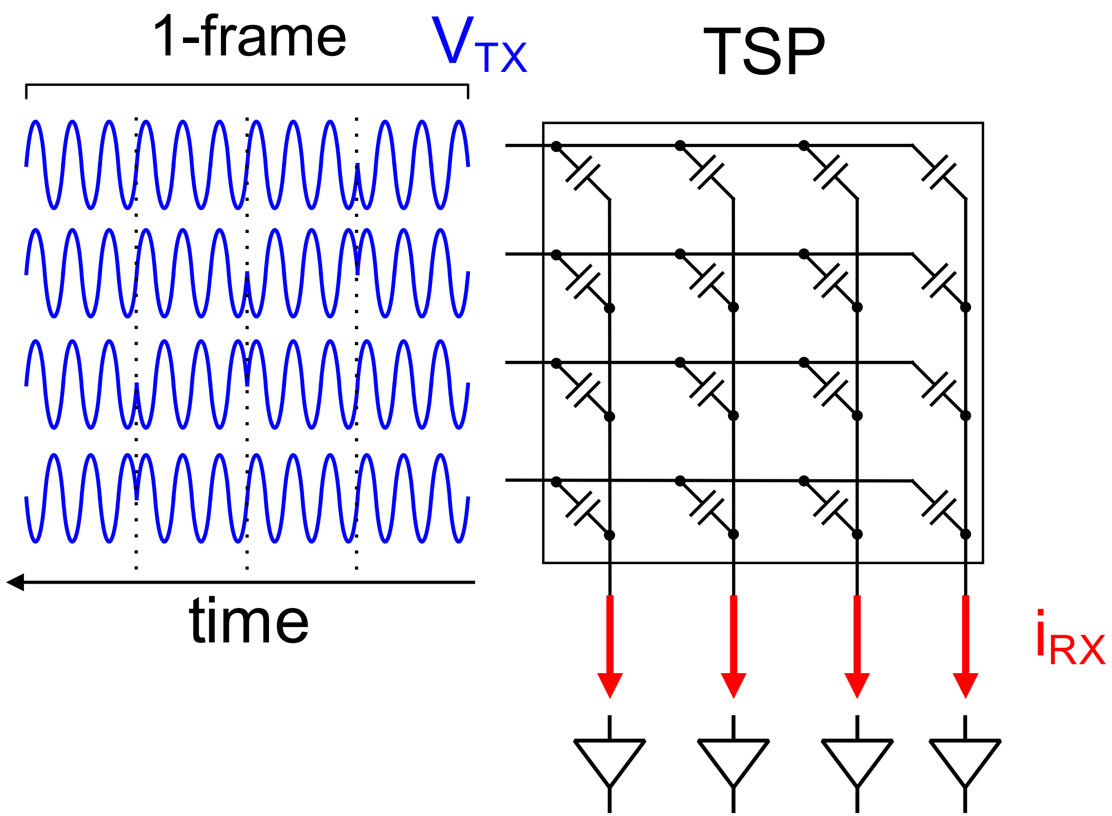
Time-interleaved TX

- Time-interleaved TX driving [3]
  - Limits access-time per node

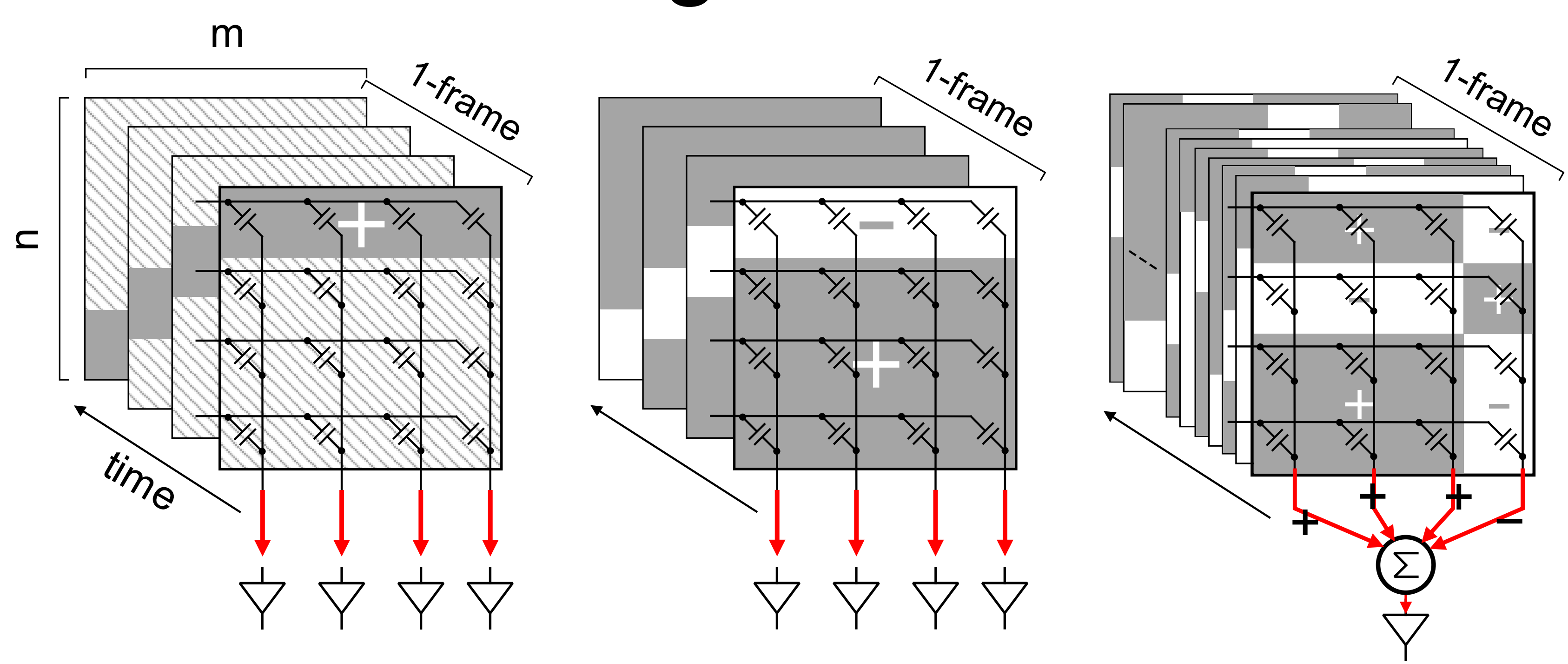


Multiple-Accessed TX

- CDMA TX [4]
  - Coded TX by phase of AC driving voltage
  - Eliminates access-time limit

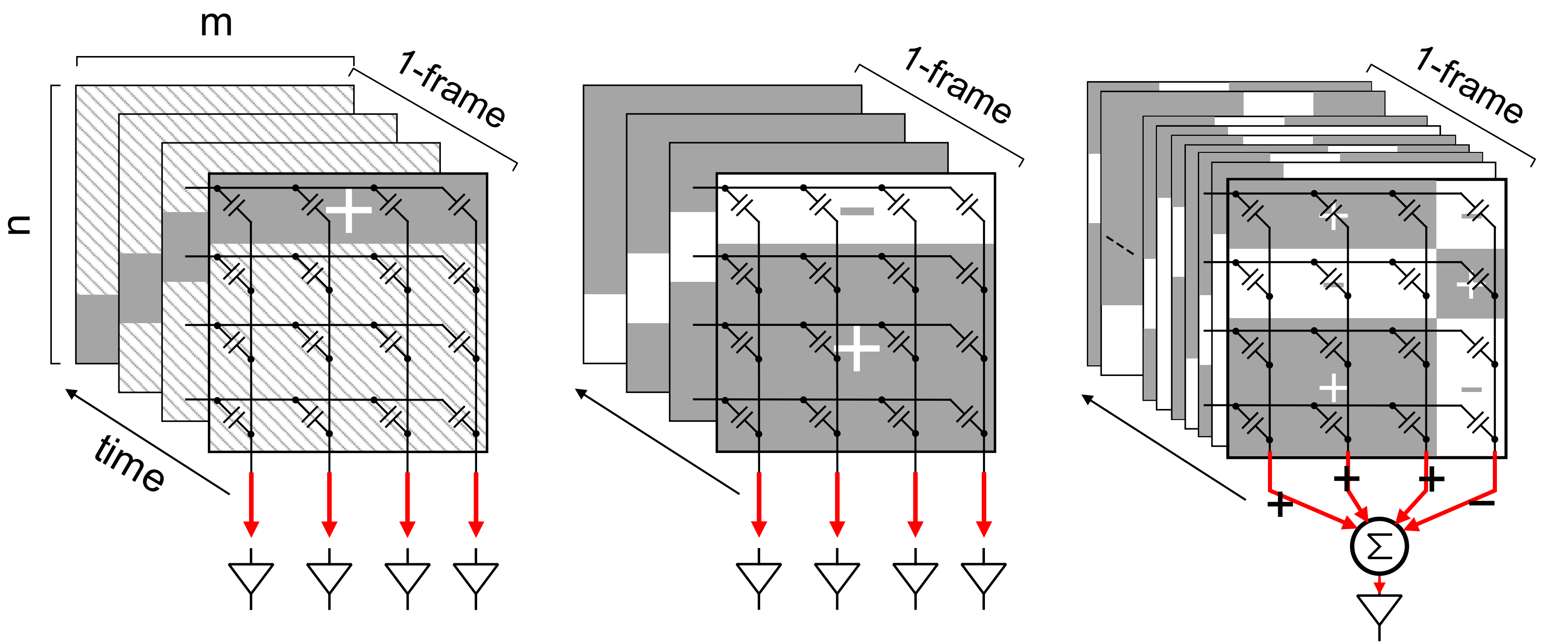


Scanning Schemes



	[2, 3]	[4]
TX	Time-interleaved	Multiple-access
RX (#CH)	Parallel (m)	Parallel (m)
Access Time	<1/n	<1

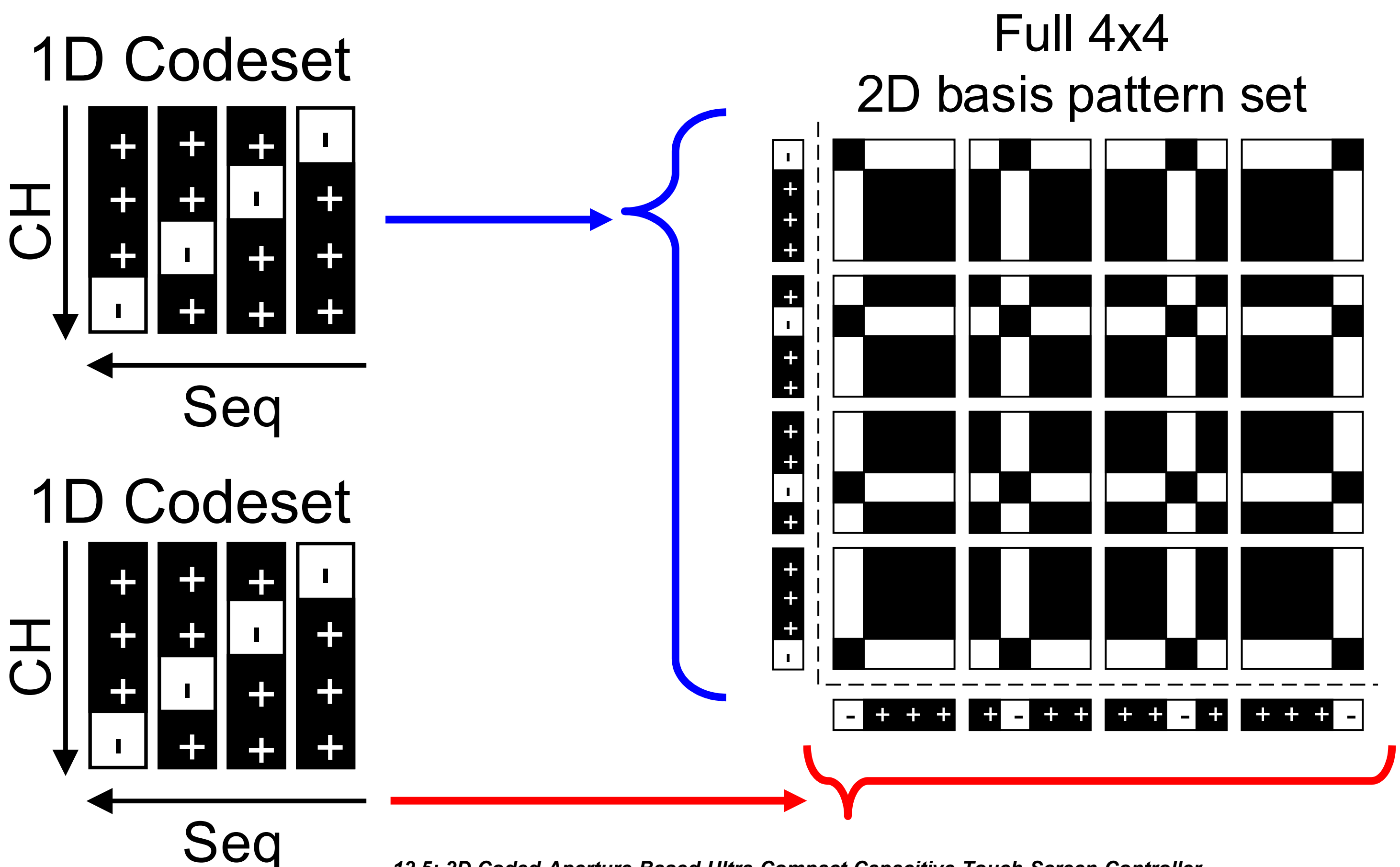
Scanning Schemes



	[2, 3]	[4]	**This work**
TX	Time-interleaved	Multiple-access	**Multiple-access**
RX (#CH)	Parallel (m)	Parallel (m)	**Multiple-access (1)**
Access Time	<1/n	<1	**<1**

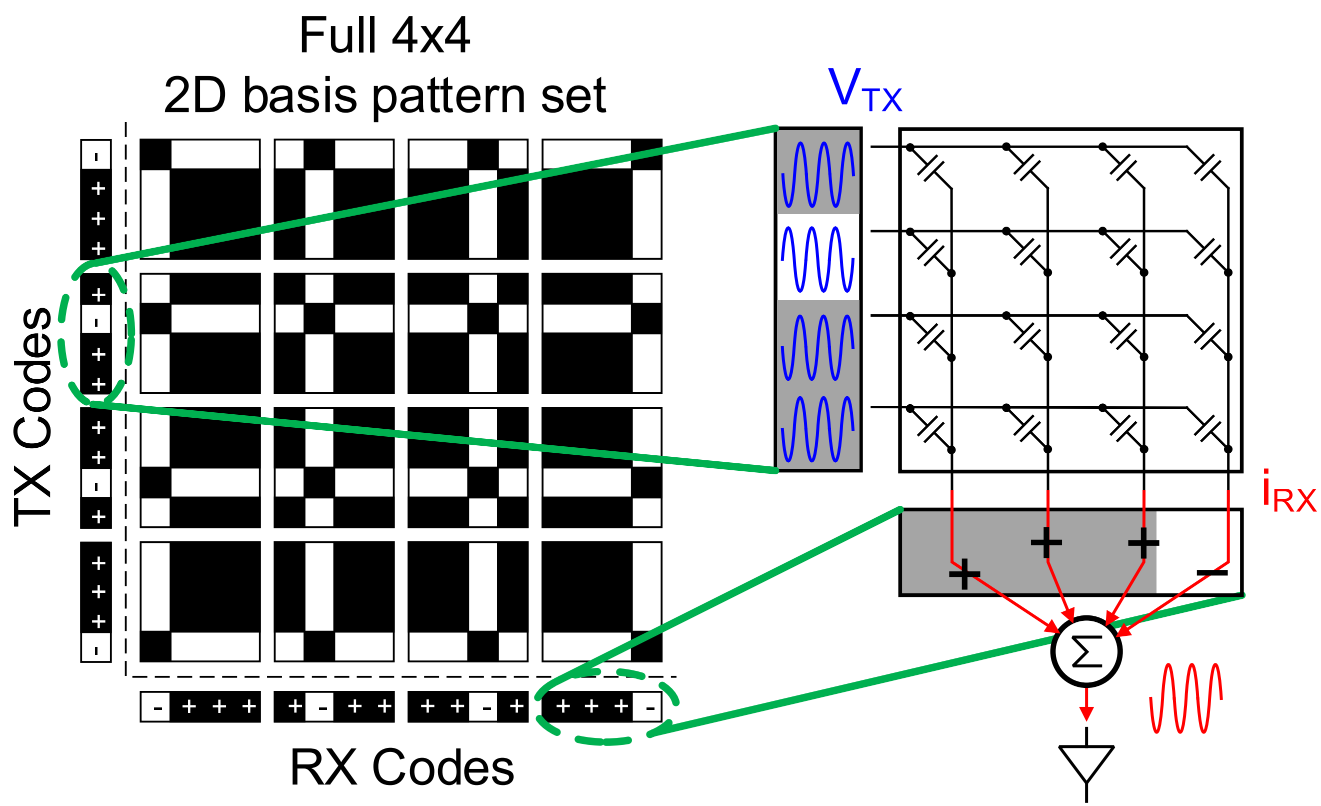
Coded-Aperture-Based Read-out

- How to project the 2D pattern?
  - 2D basis patterns can be attained by (1D Code ⊗ 1D Code)



Coded-Aperture-Based Read-out

- How to project the 2D pattern?
  - TX Code: AC driving phase
  - RX Code: RX current summing polarity



Coded-Aperture-Based Read-out

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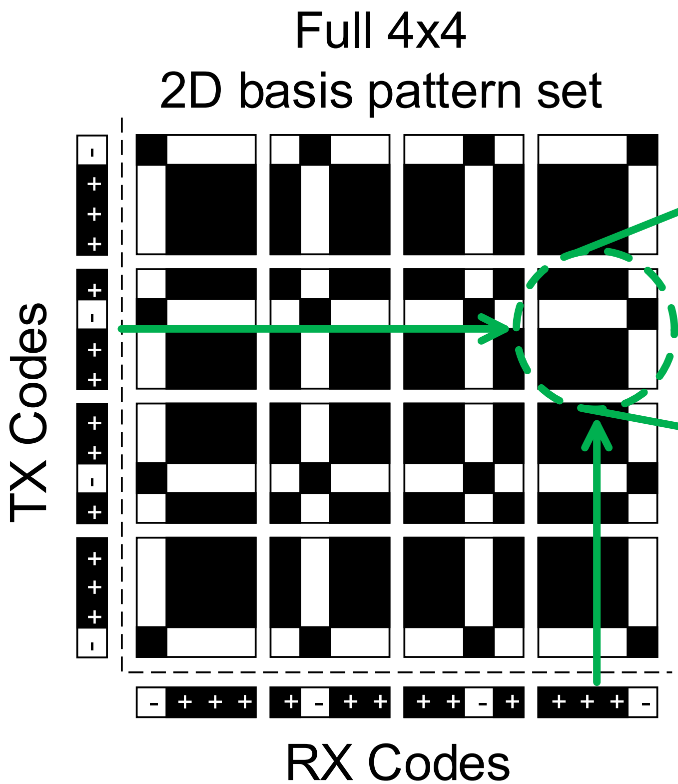
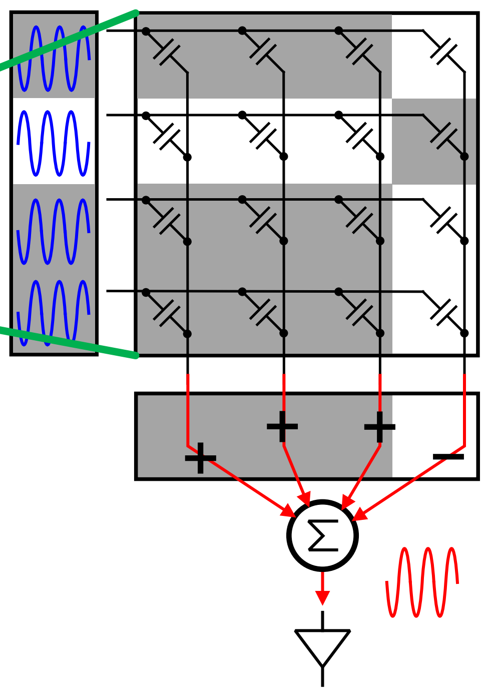
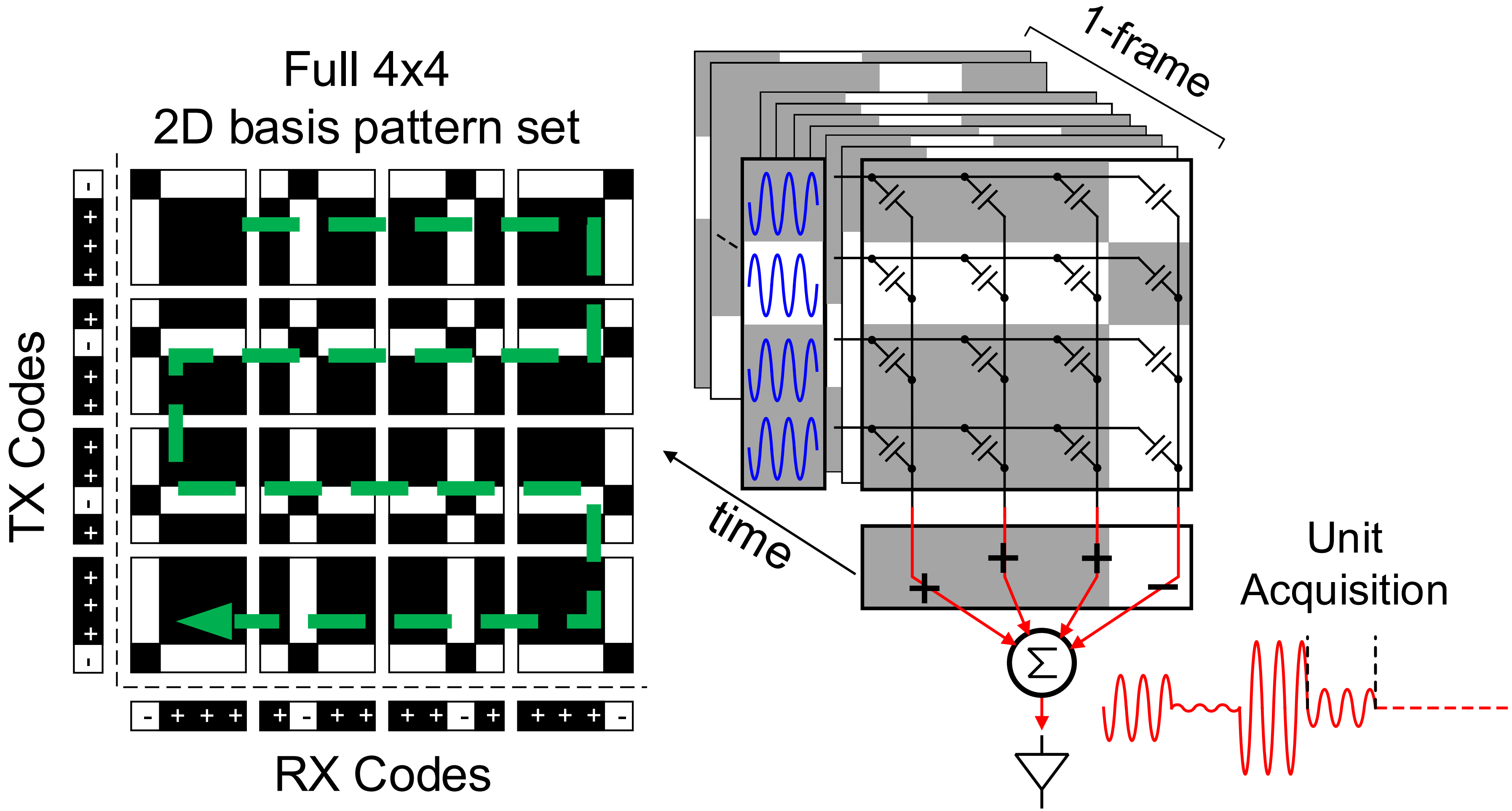




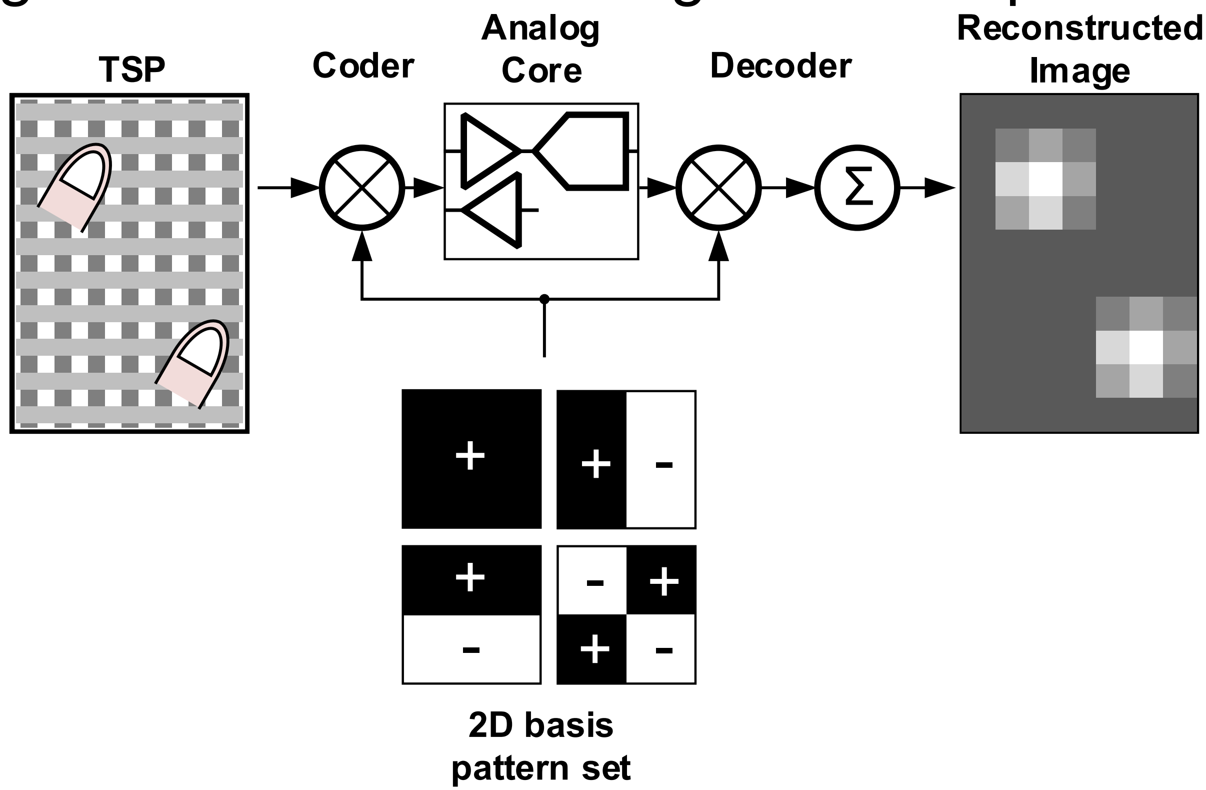
Coded-Aperture-Based Read-out

- Repeat for whole set to fully specify



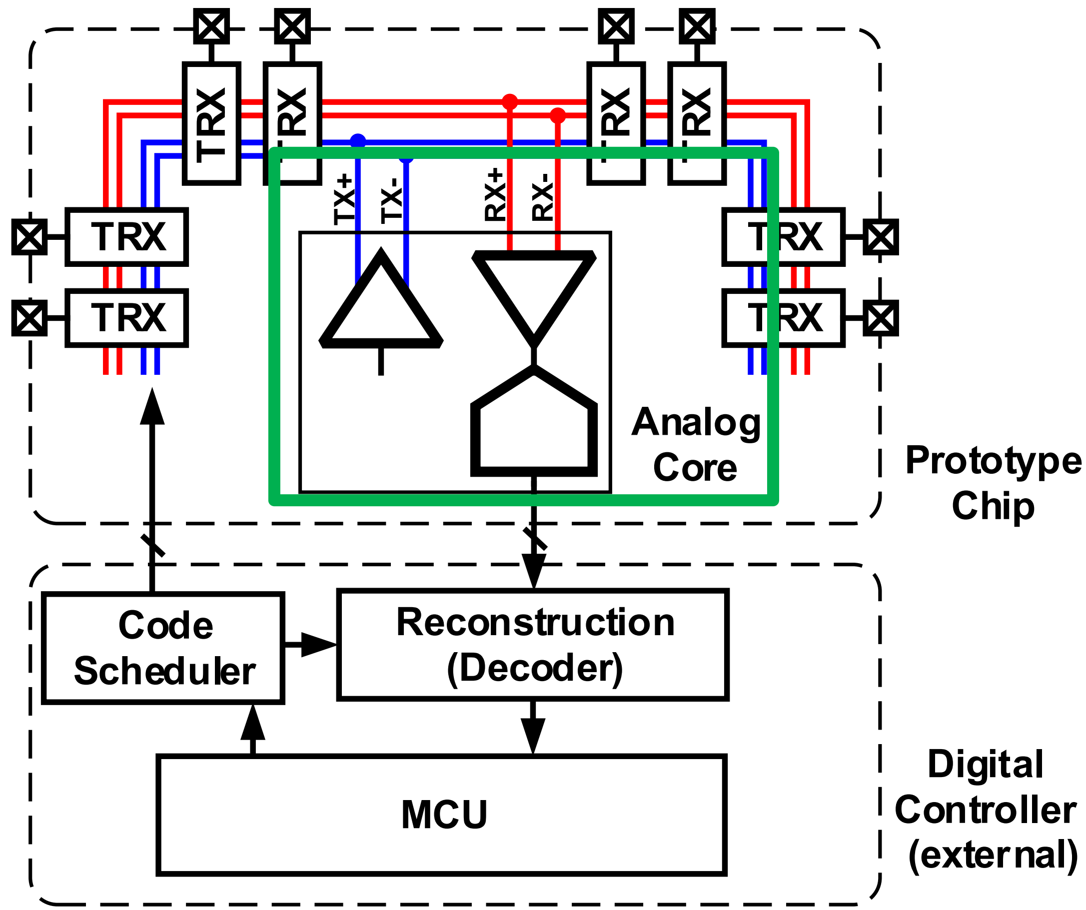
Coded-Aperture-Based Read-out

- Whole system
  - Acquisition in response to 2D basis patterns
  - Sensing it using single-channel analog core
  - Digital reconstruction using the same patterns



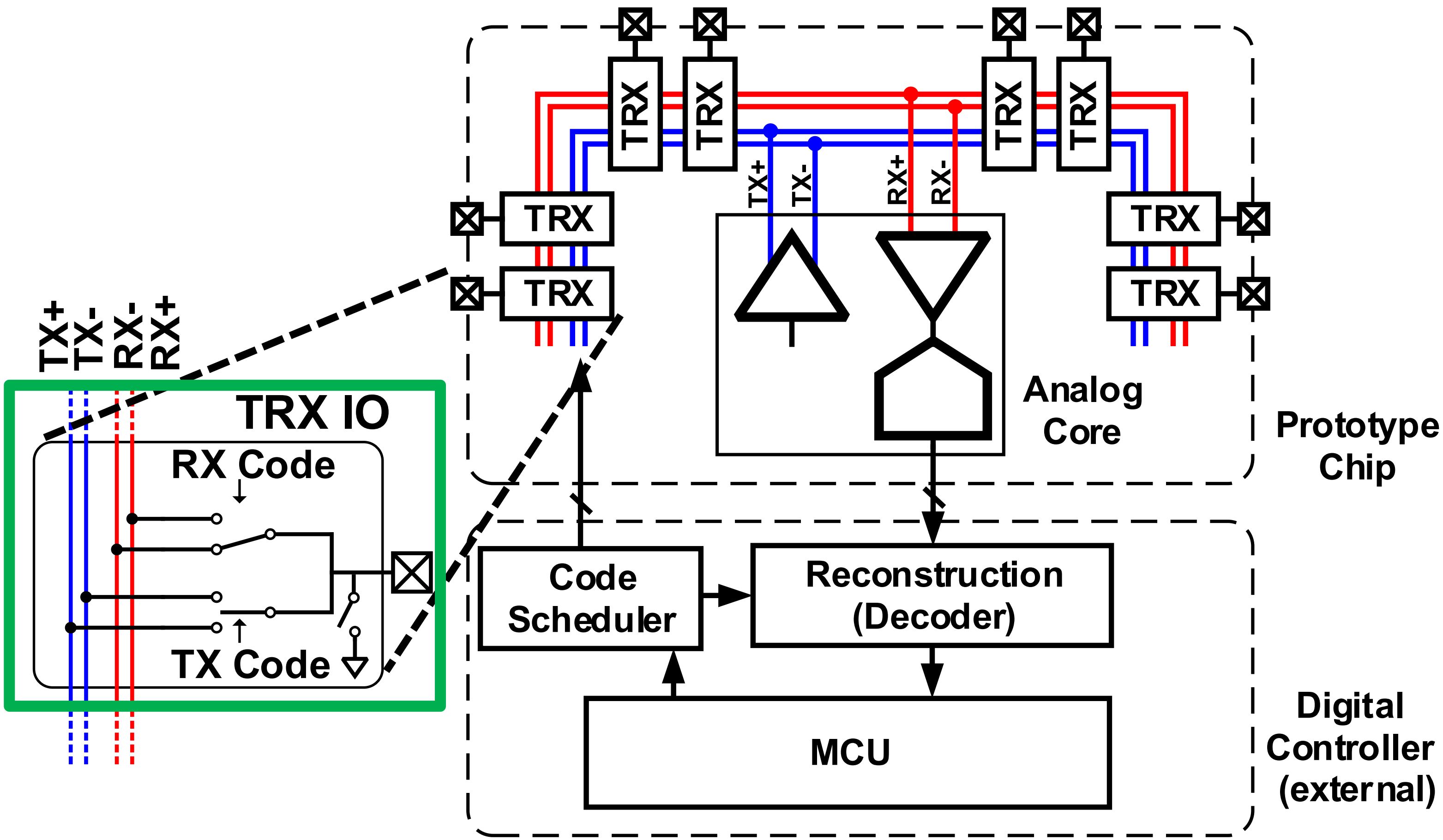
Architecture Implementation

- Analog core: TX core + RX core



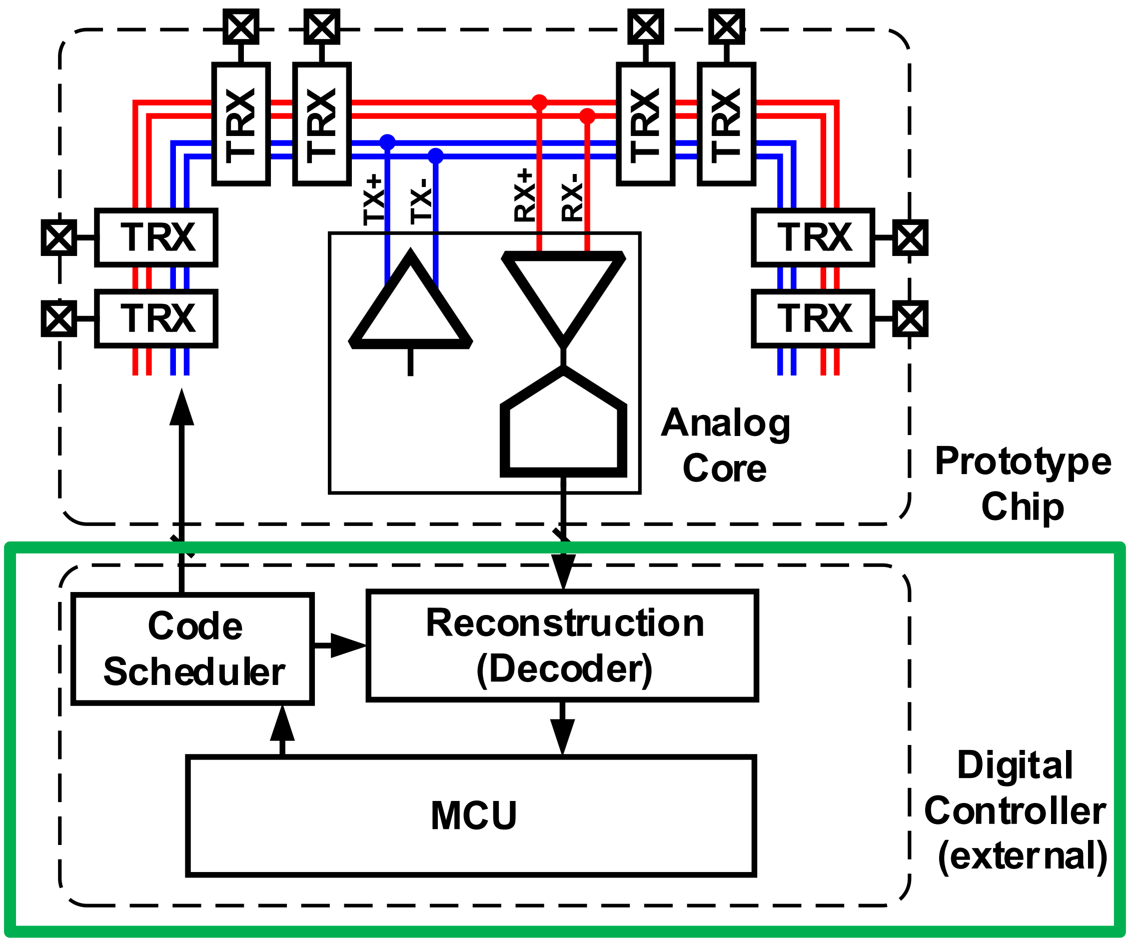
Architecture Implementation

- Reconfigurable TRX I/Os on shared TX/RX ring
  → Reconfigurable & scalable channels



Architecture Implementation

- Digital controller
  - Code schedule, reconstruction, and feature extraction

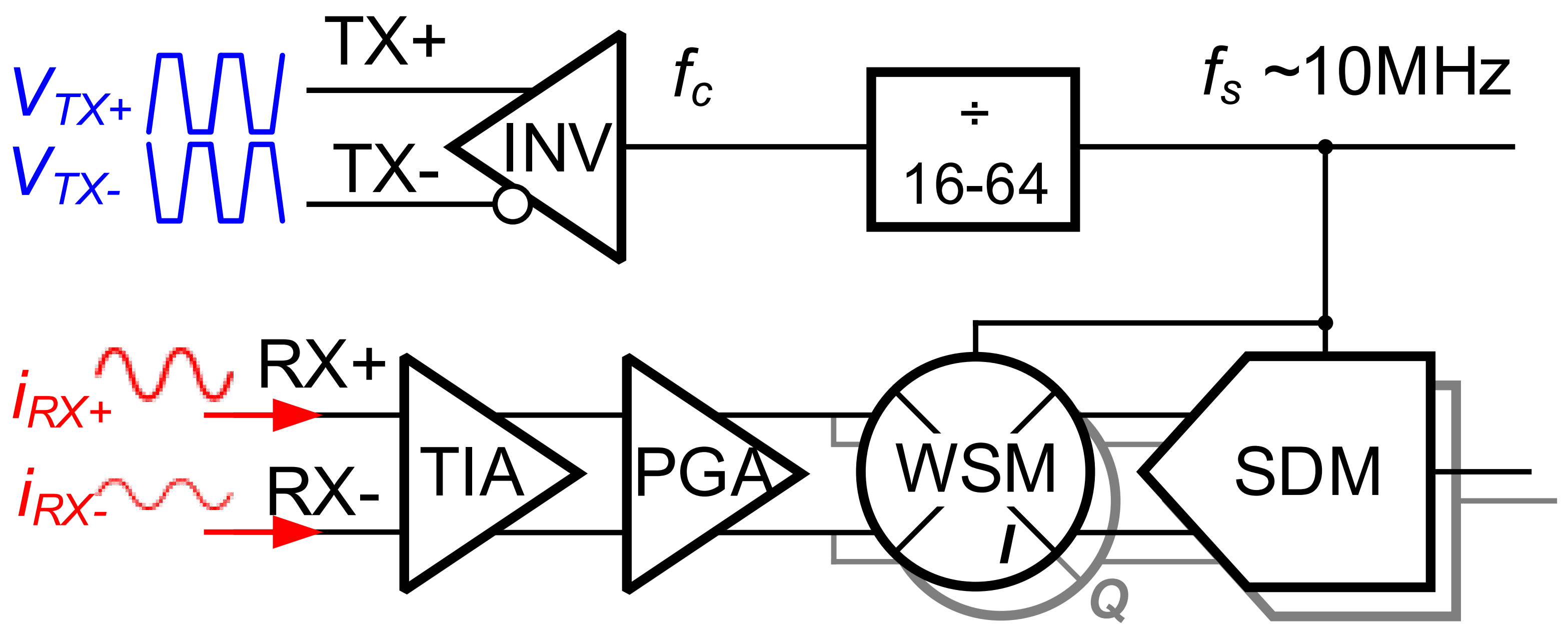


Outline

- Introduction & Motivation
- Coded-aperture-based Read-out
- Circuit Design Details
  - TIA and offset minimization
  - WSM and harmonic rejection
  - Delay-loss compensation
- Experimental Results
- Summary and Conclusion

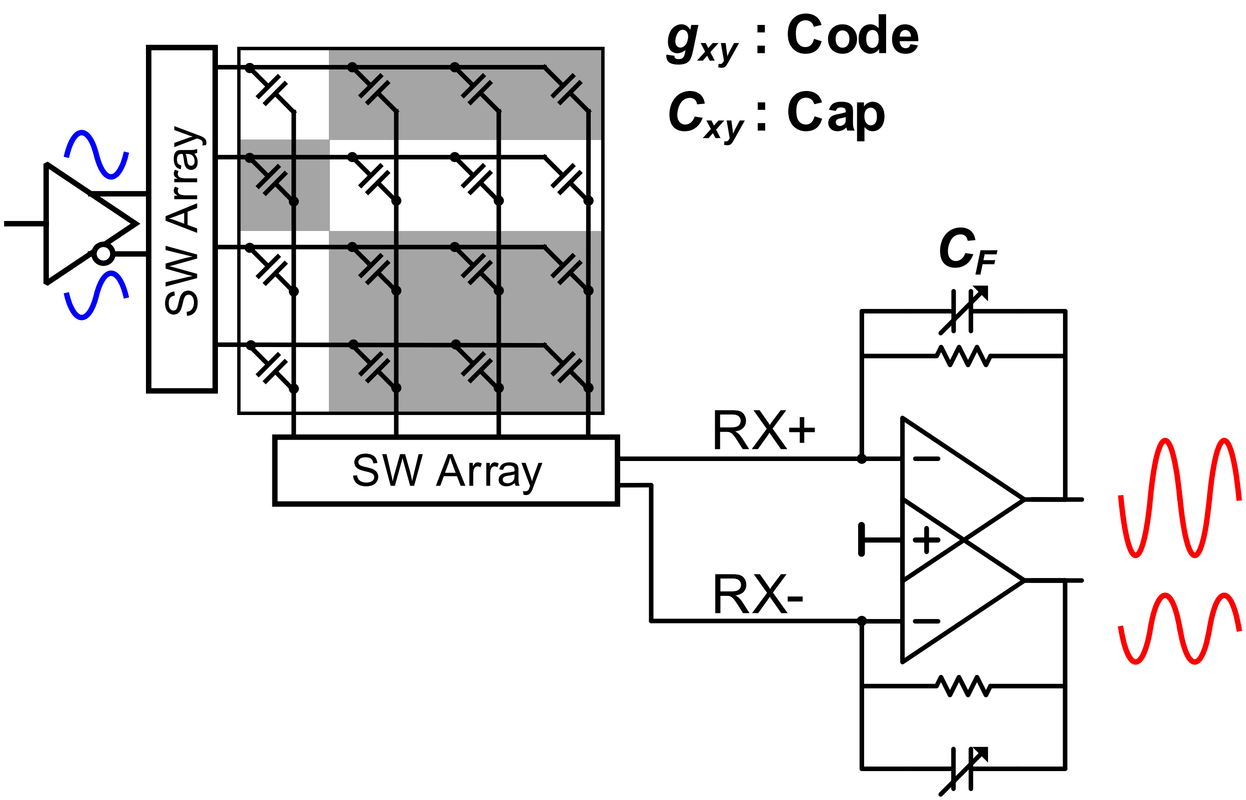
Analog Core

- TX: differentially driven slew-limited inverters
- RX: TIA, PGA, Mixer, and SDM
  - Converts the amplitude of AC signal currents into digital data with robust signal-conditioning



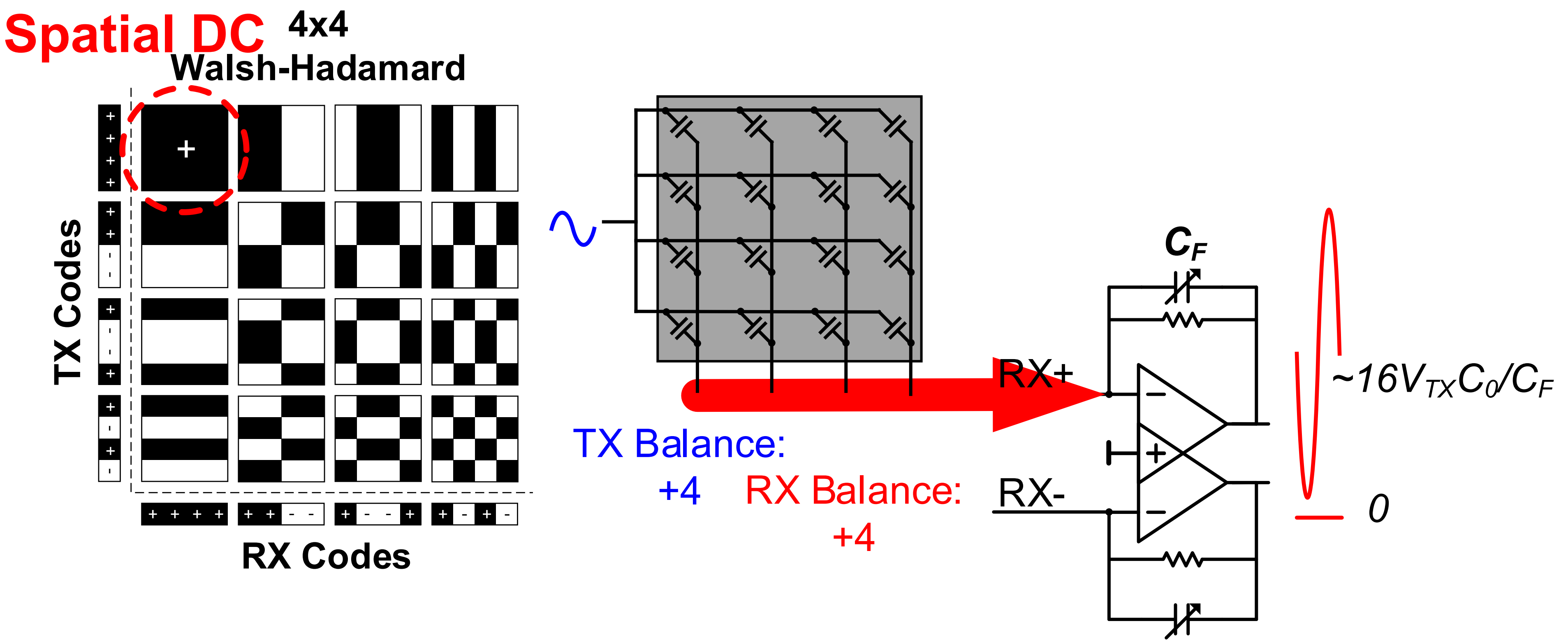
Front-end TIA

- Pseudo-differential TIAs with C_F
  - Provides low-Z and converts I-V
  - Bandpass TF of $A_0 \sim (\Sigma g_{xy} C_{xy} / C_F)$
    → AC amplitude ∝ (total sum of coded capacitance)



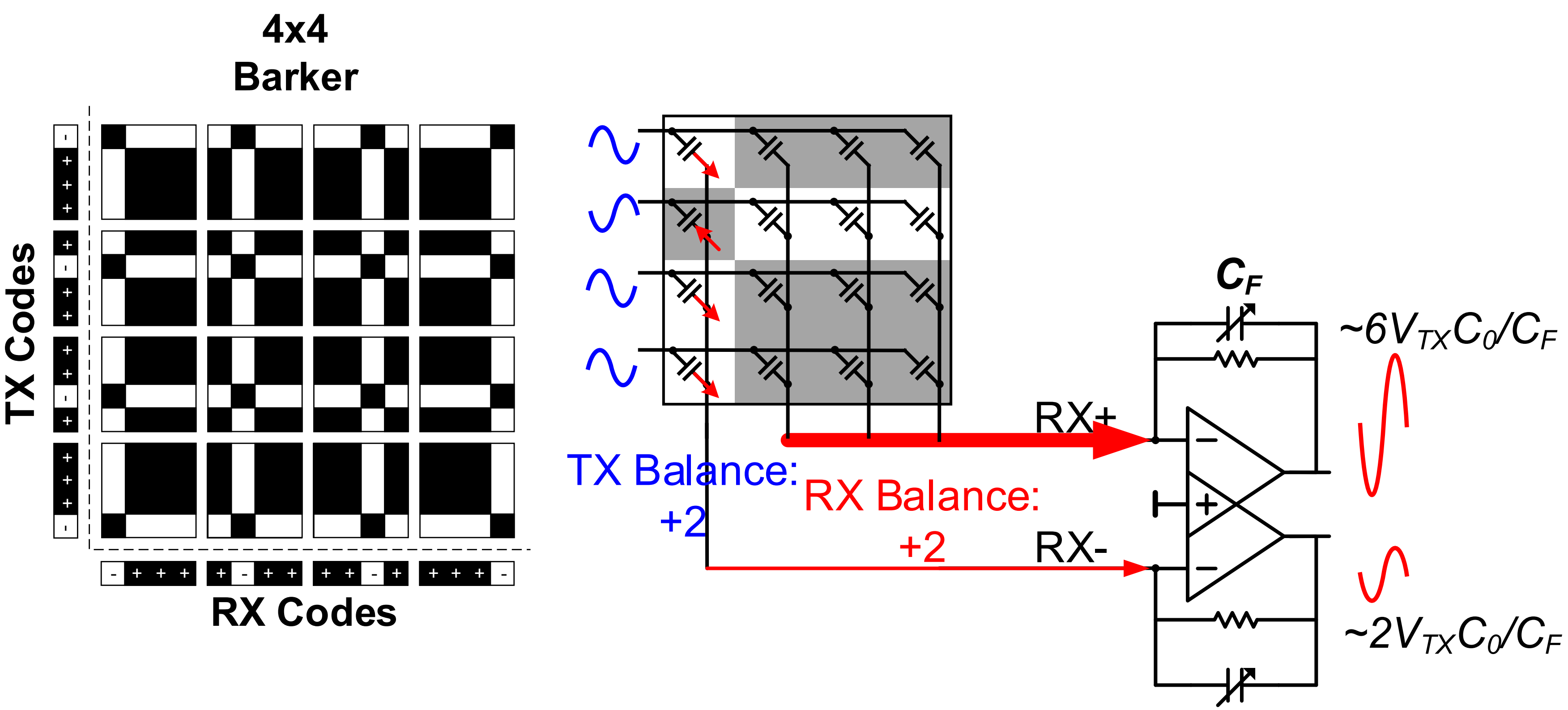
Front-end TIA

- Offset problem
  - $C_{XY} \sim (C_0+\Delta C) \sim C_0 \sim 1pF \rightarrow$ AC-offset current
  - May need huge C_F



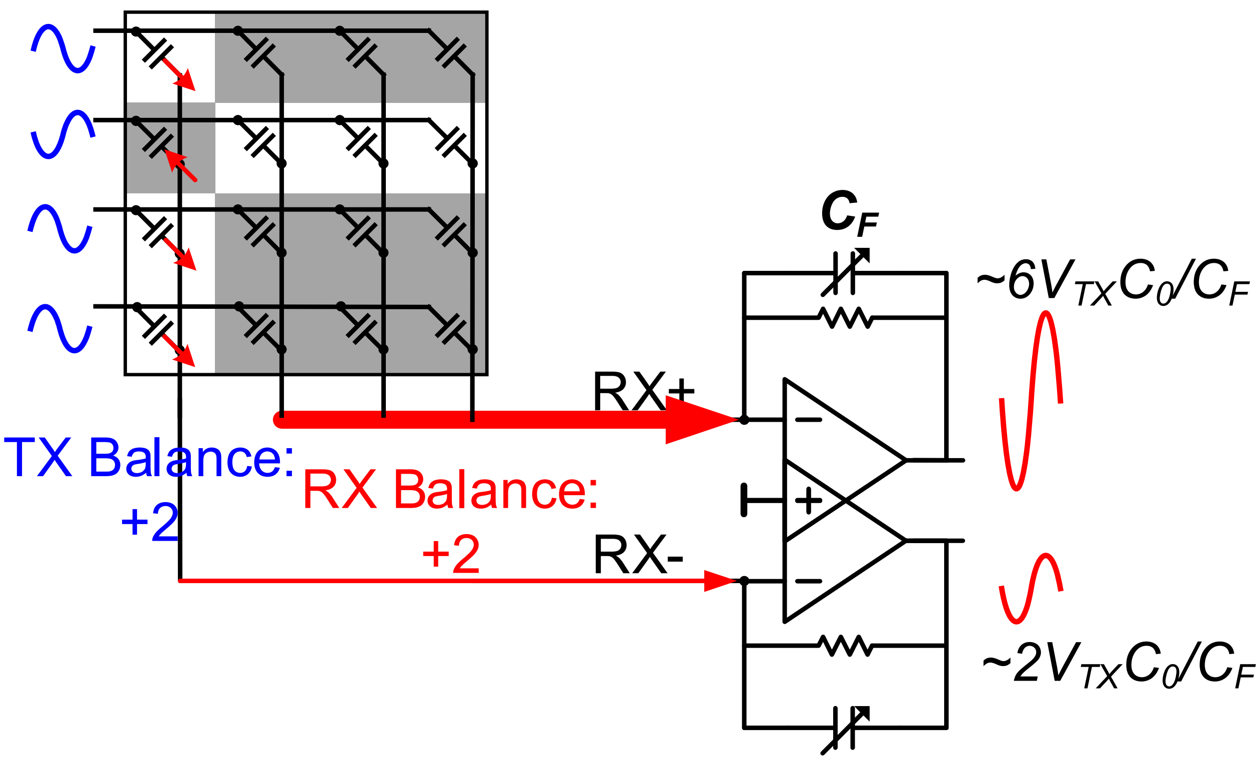
Front-end TIA

- Offset problem
  - Using well-balanced code lets AC-offset currents cancel each other



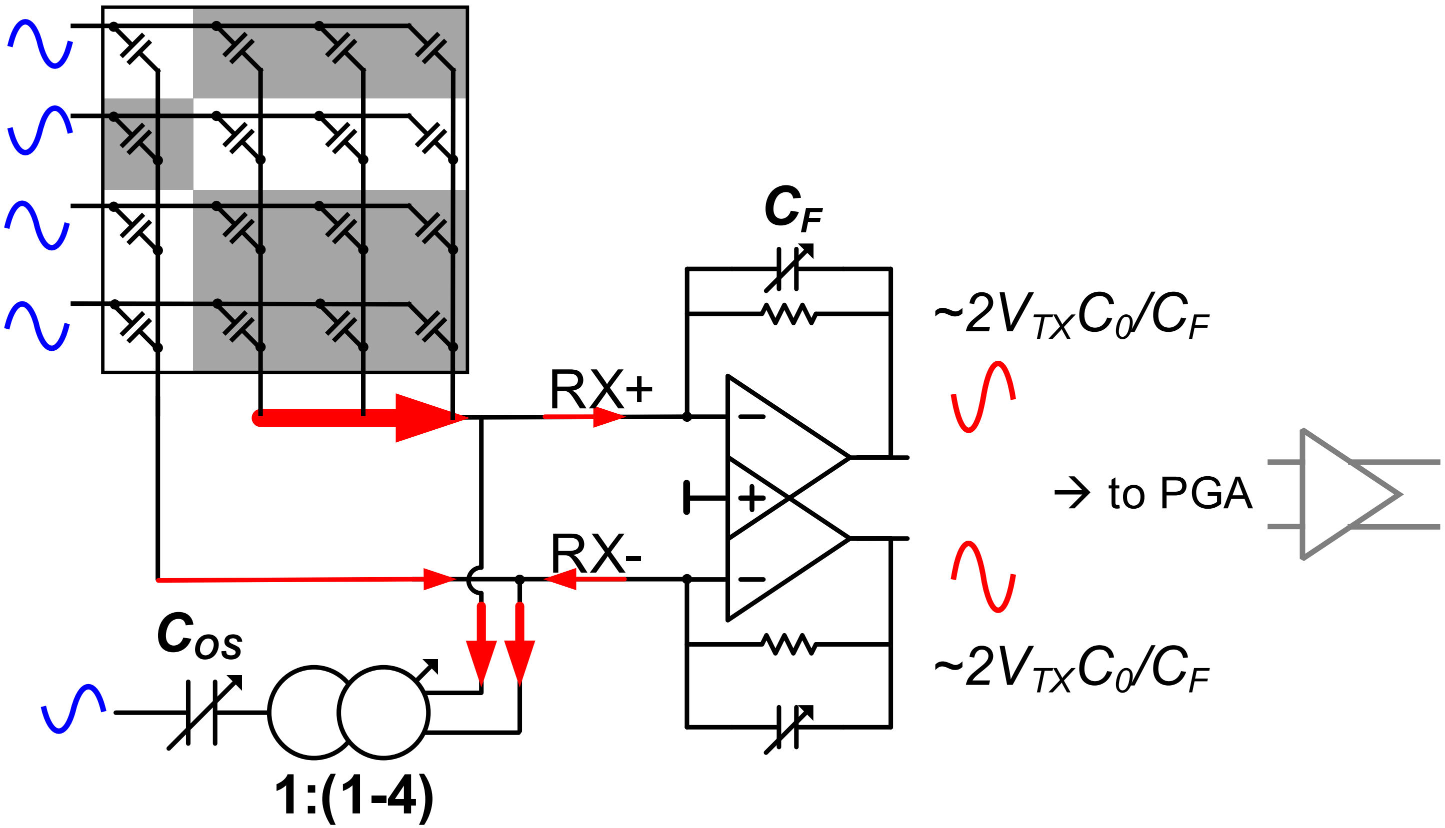
Front-end TIA

- Still large swing since
  - (Orthogonality ←→ Balance) for binary code
  - C_0 mismatch and panel RC-delay breaks balance



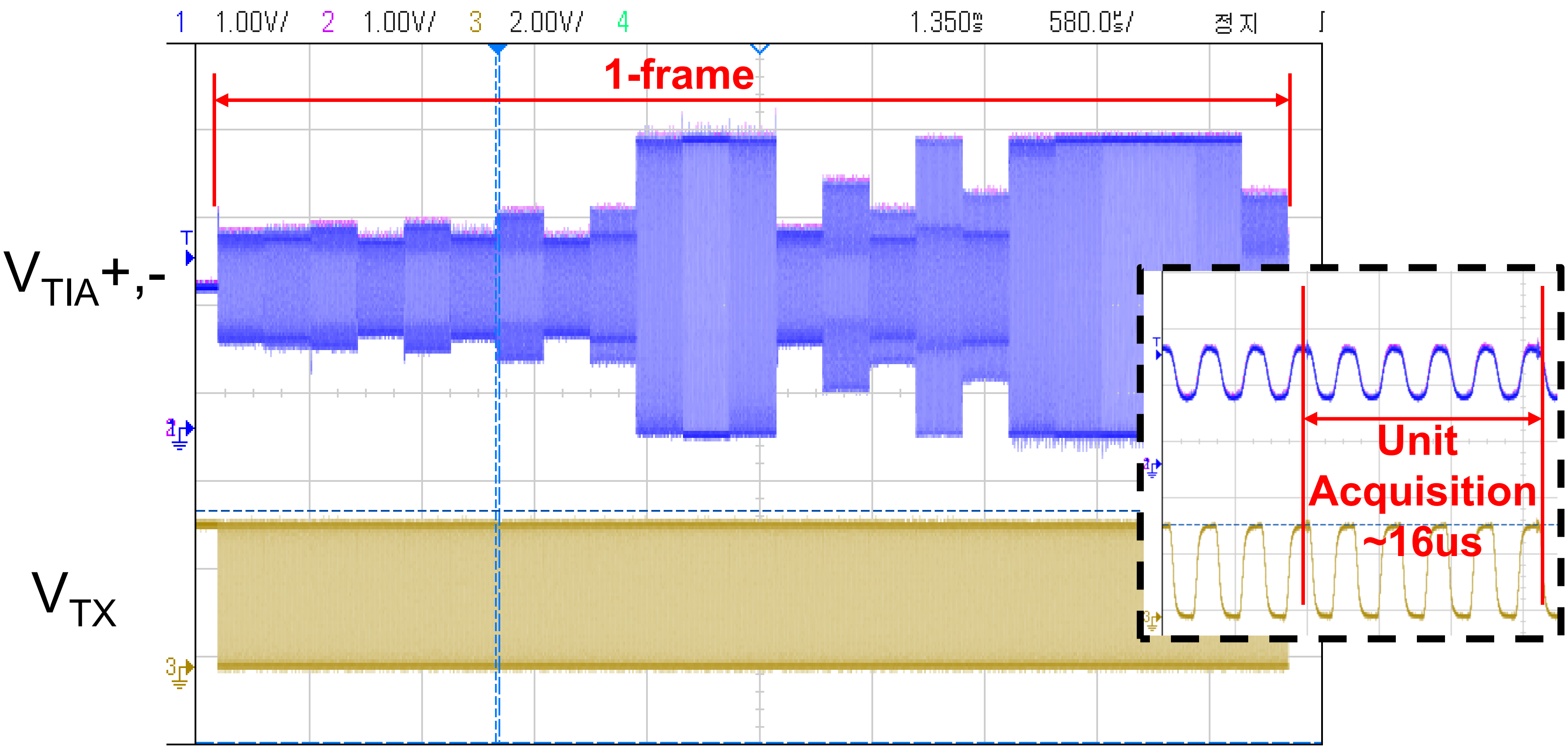
Front-end TIA

- OS Canceller
  - C_{OS} + Current-scaler
  - Injects boosted common-mode cancelling current



Front-end TIA

- Measurement results
  - 24-TX$_X$16-RX TSP, f_c=312kHz
  - Unbalanced code, without OS canceller



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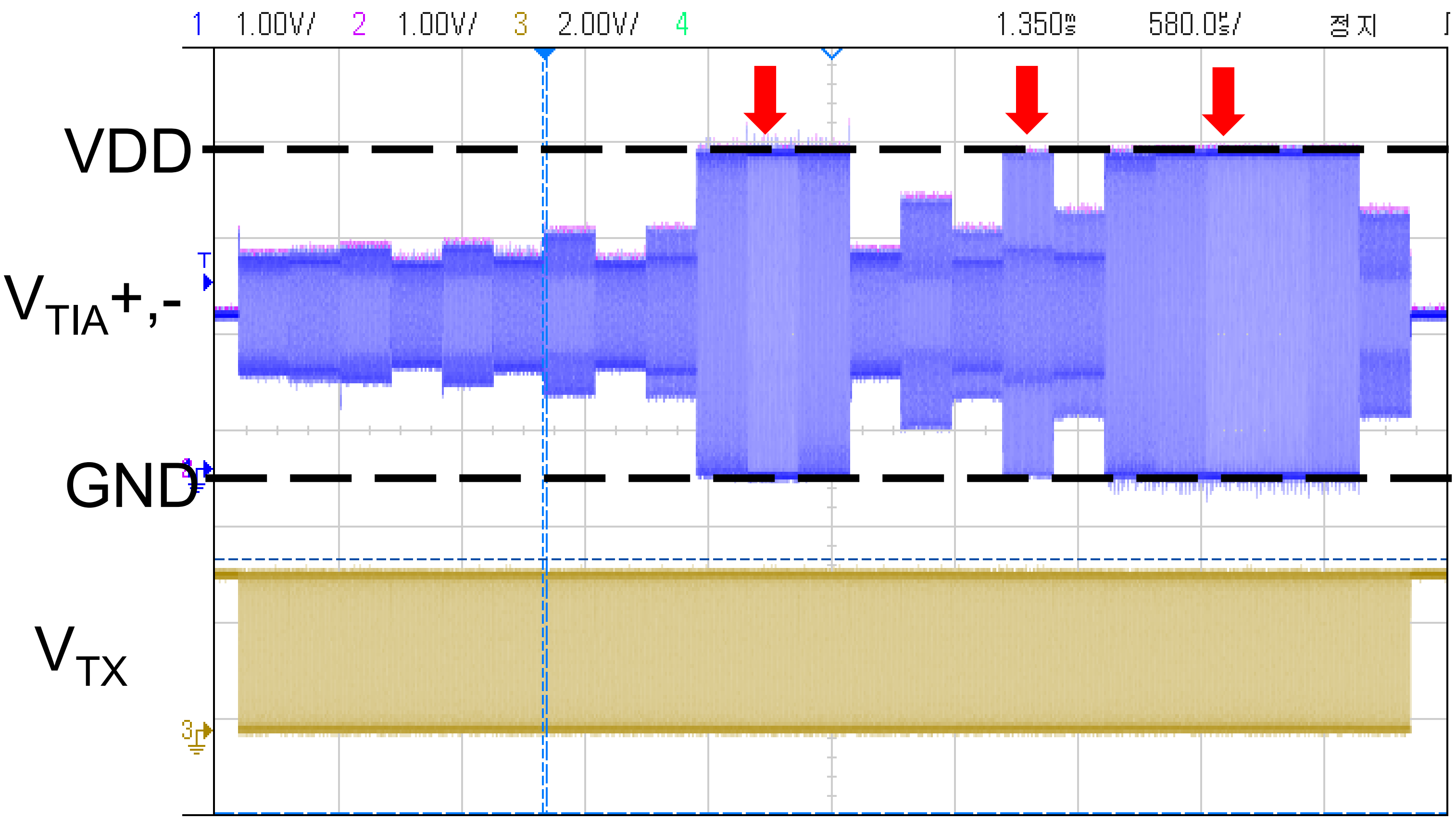
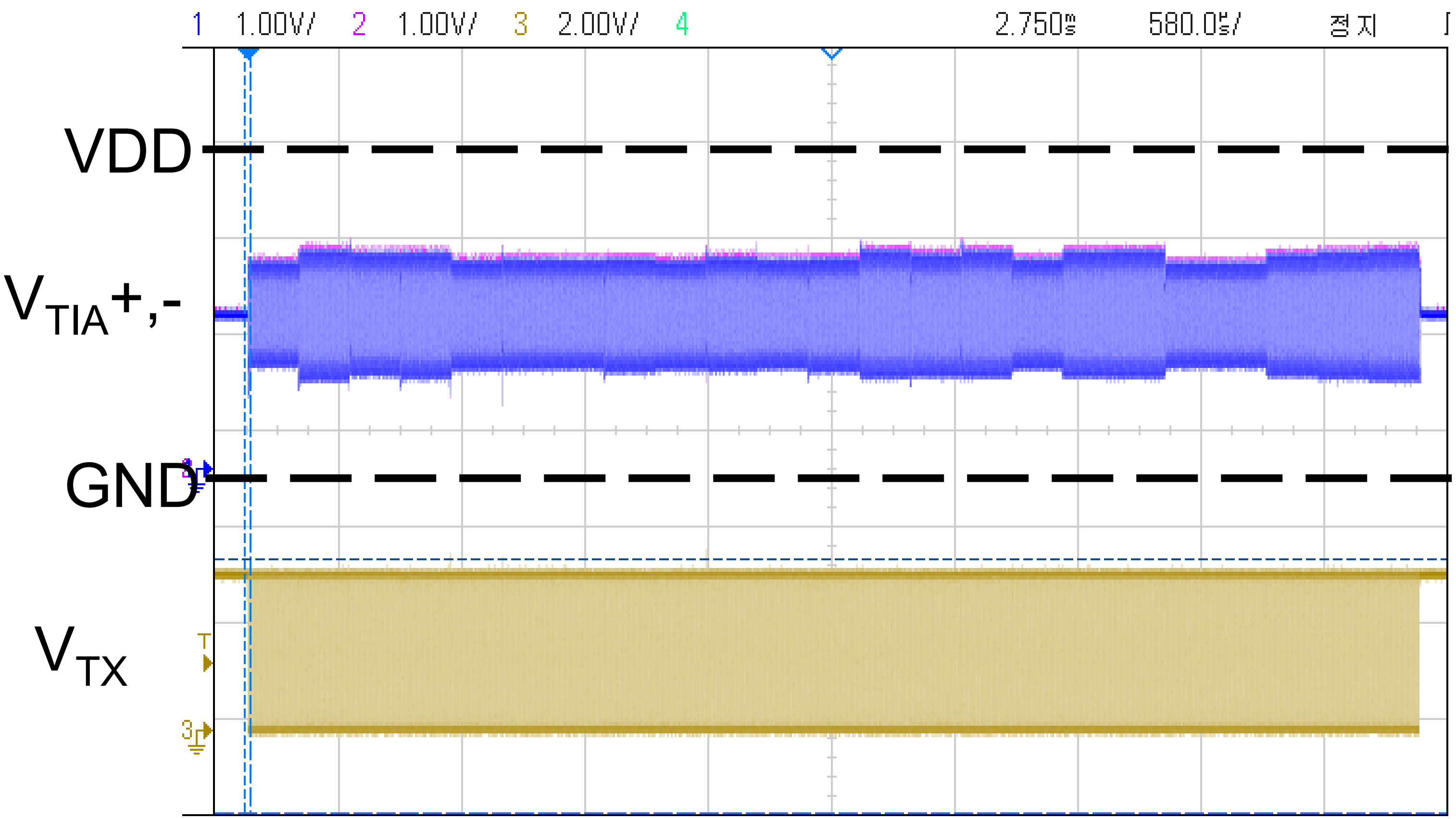


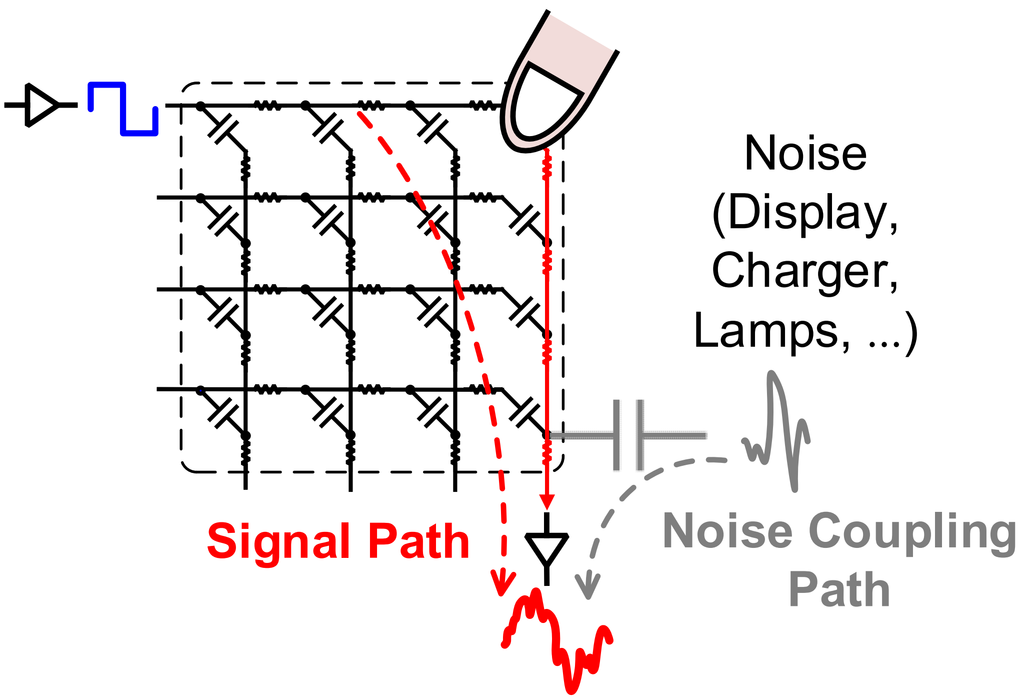
Front-end TIA

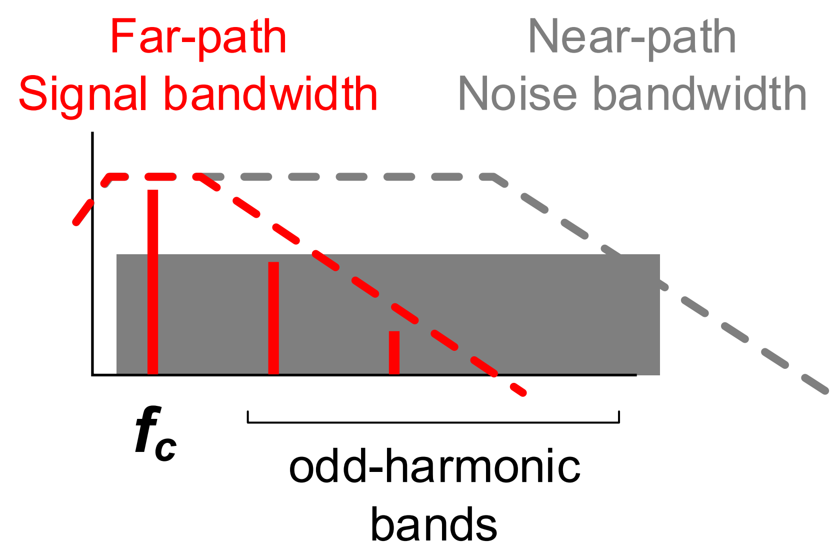
- Measurement results
  - Balanced code, with OS canceller



Down-mixing Consideration

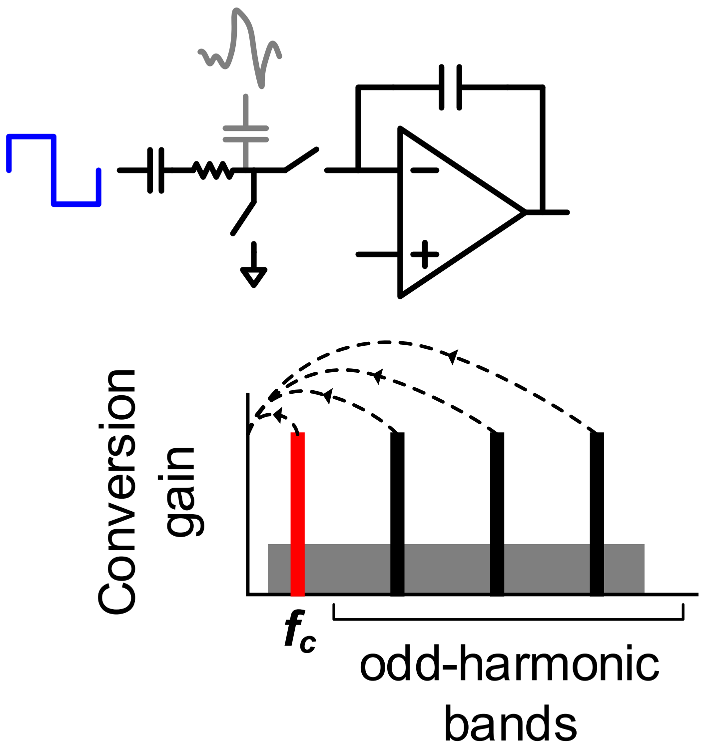
- Signal is band-limited
- Noise couples through wide-band

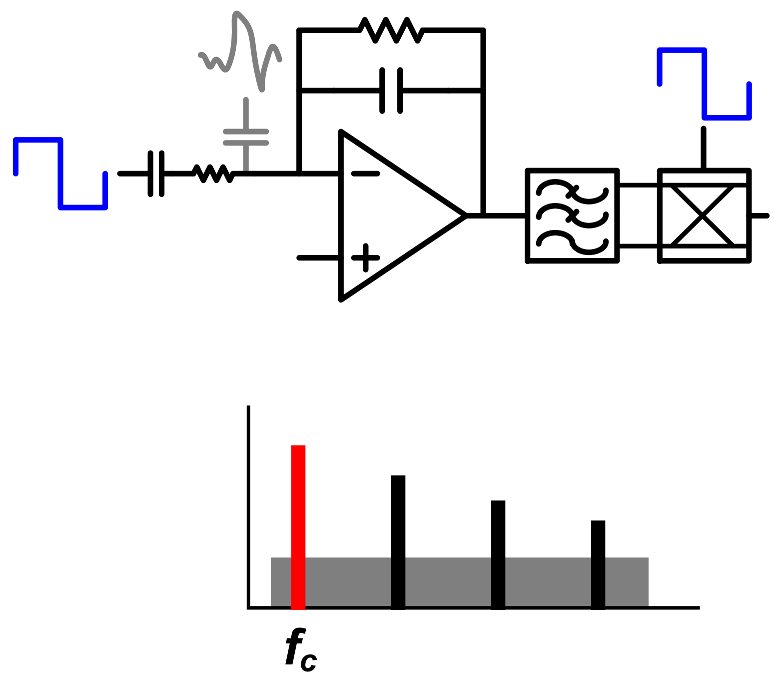




Down-mixing Circuit Comparison

- Switched-Capacitor [4]
- Square-wave Mixing [3]



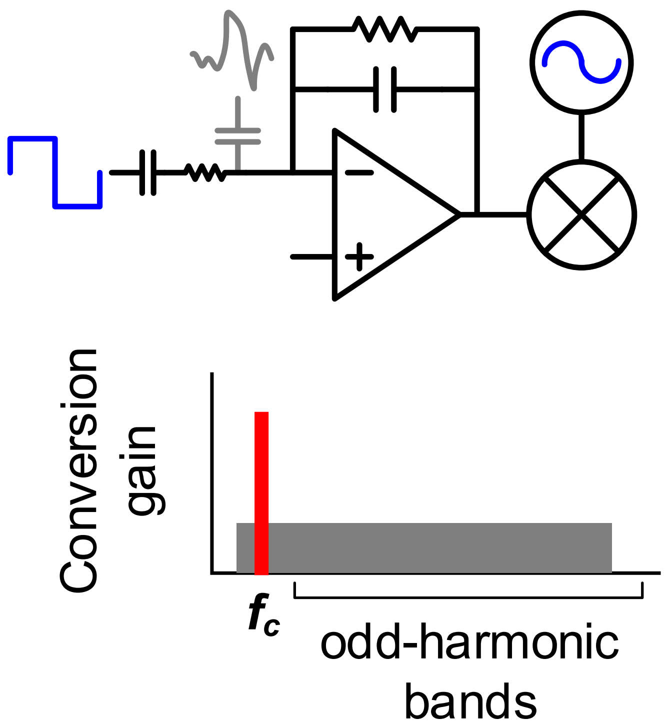


+Simple
- Aliasing

+Filter applicable
- Filter complexity

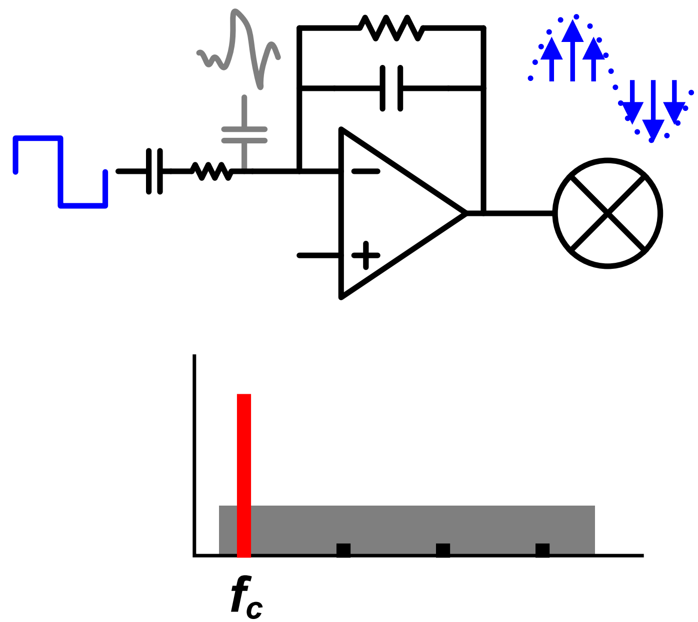
Down-mixing Circuit Comparison (cont'd)

- Sinusoidal Mixing [2]



+Harmonic band rejection
- Complex and active

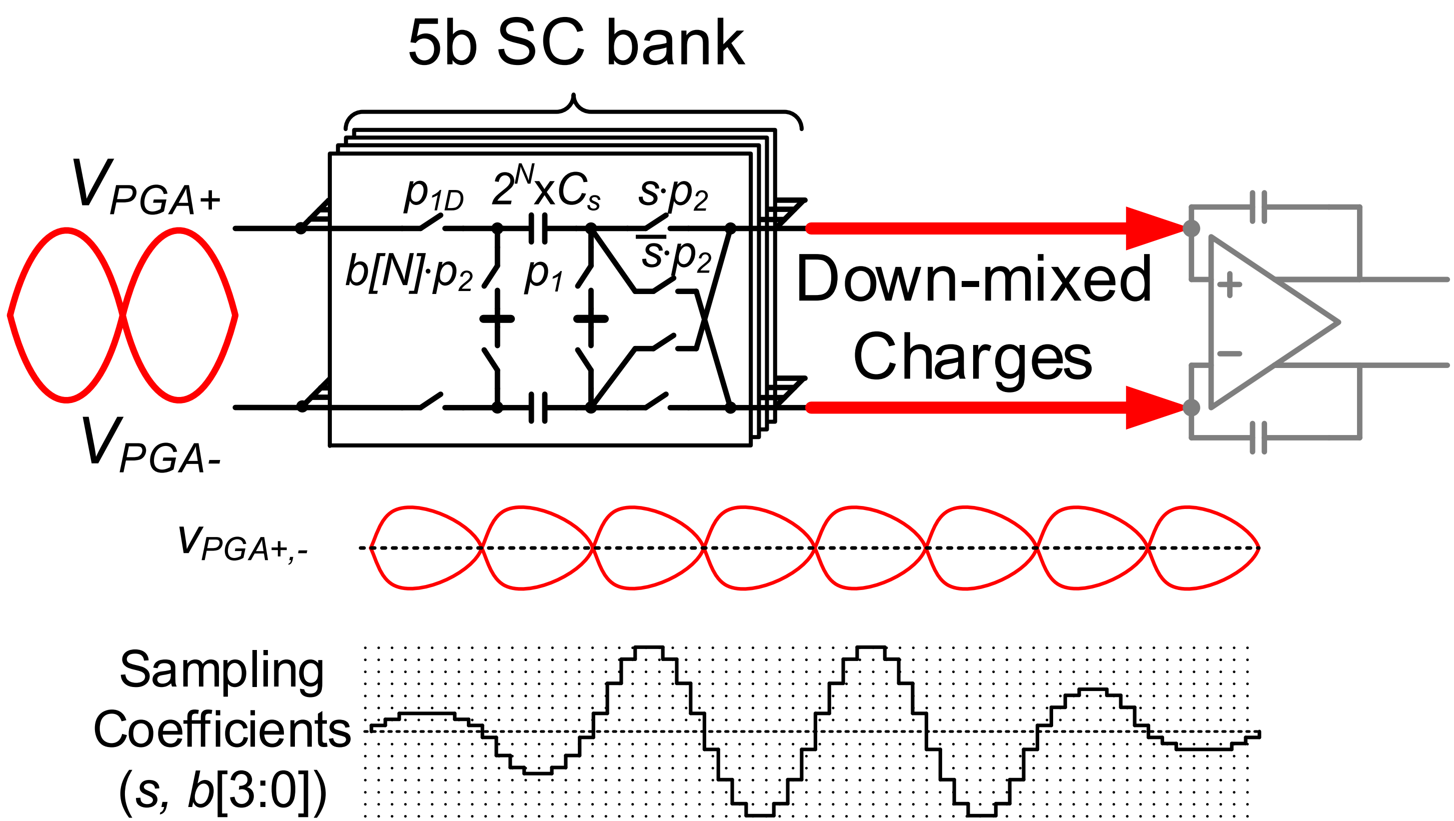
- Wave-shaping [This work]



+Harmonic band rejection
+Fairly simple

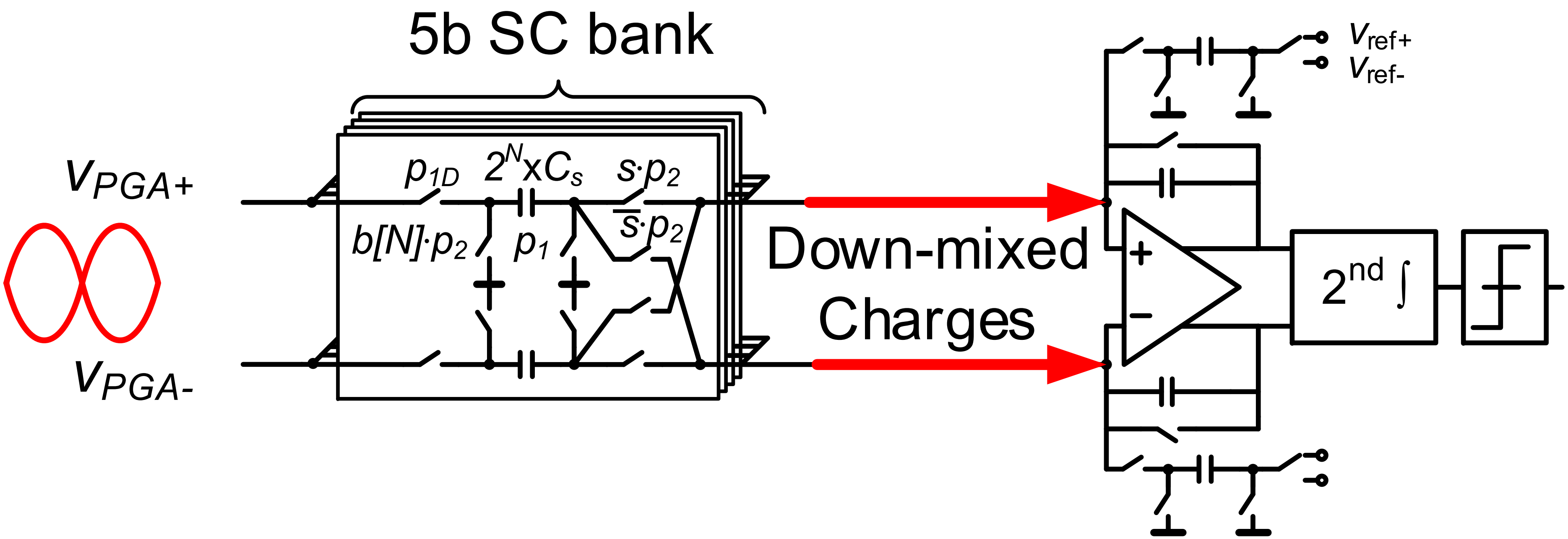
Wave-shaping Mixer

- Shaped sampling coefficients using SC network
  - @p_1: Fully-charge
  - @p_2: Partially transfer through chopper



Wave-shaping Mixer + SDM

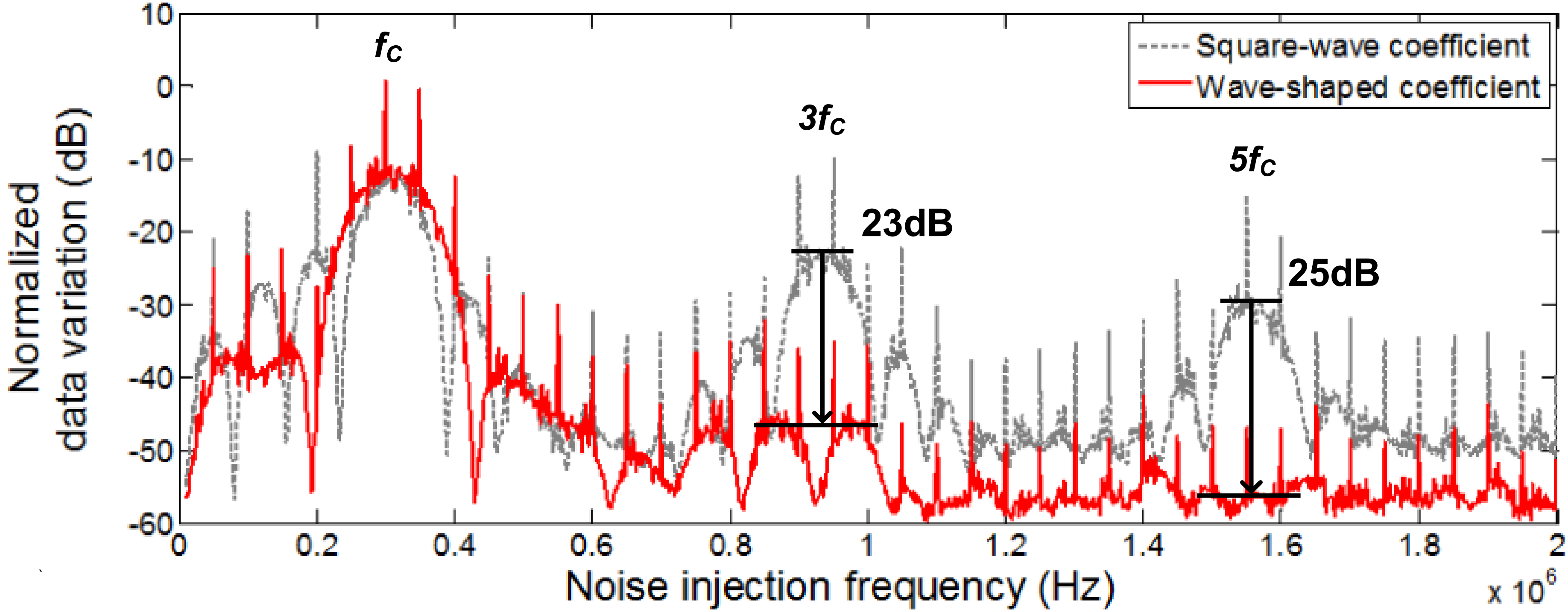
- Connecting to SDM 1st integrator
  - Mixer also working as SDM input capacitor



Wave-shaping Mixer + SDM

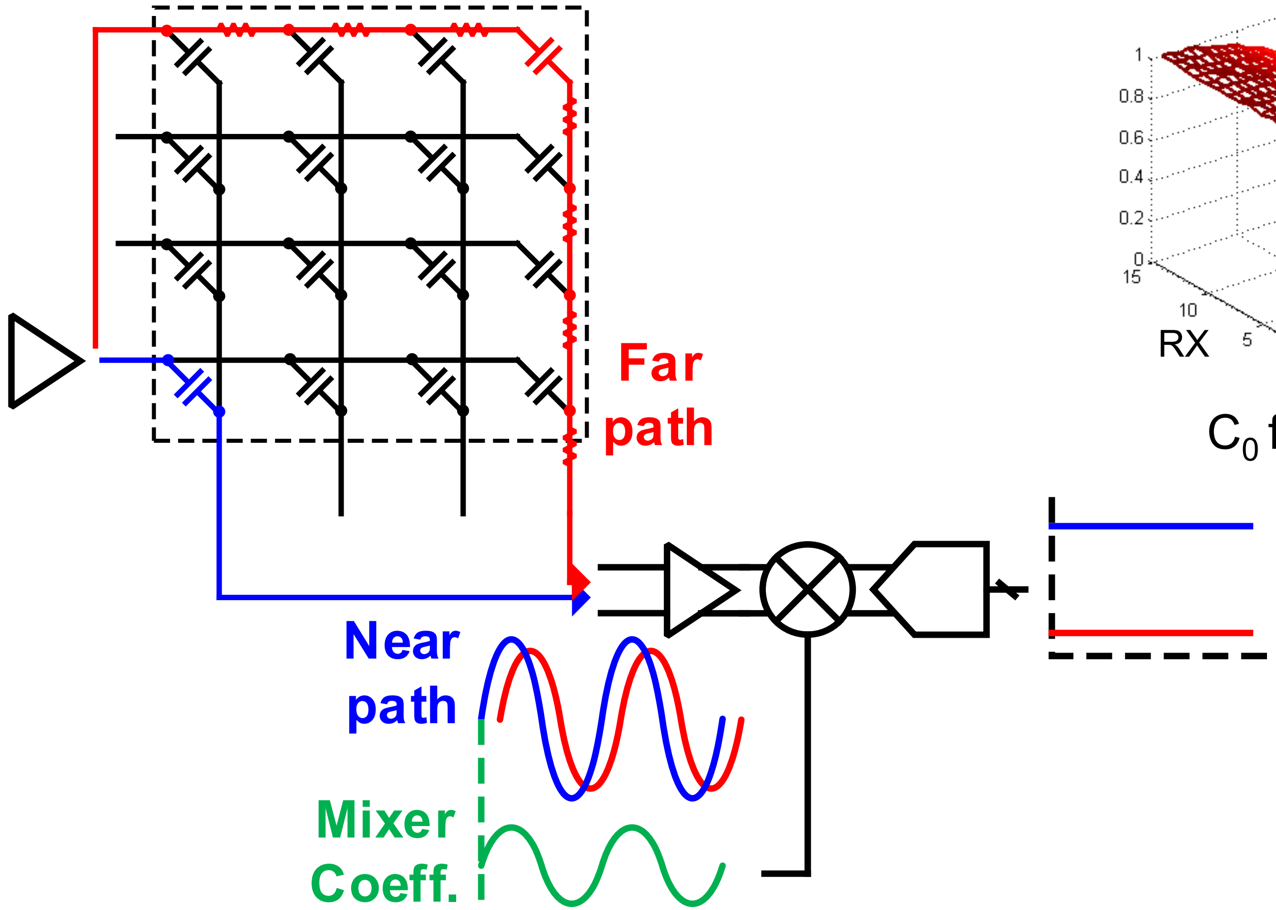
- Measurement result
  – Reconstructed data variation
  by frequency-swept noise injection

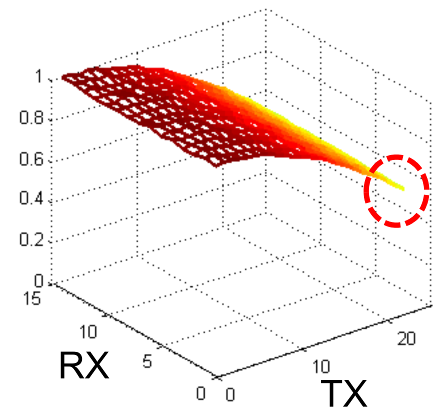
(f_s=10MHz, f_c=312kHz)



Delay-loss Compensation

- Different phase delays due to panel RC
  → Signal loss at down-mixing stage

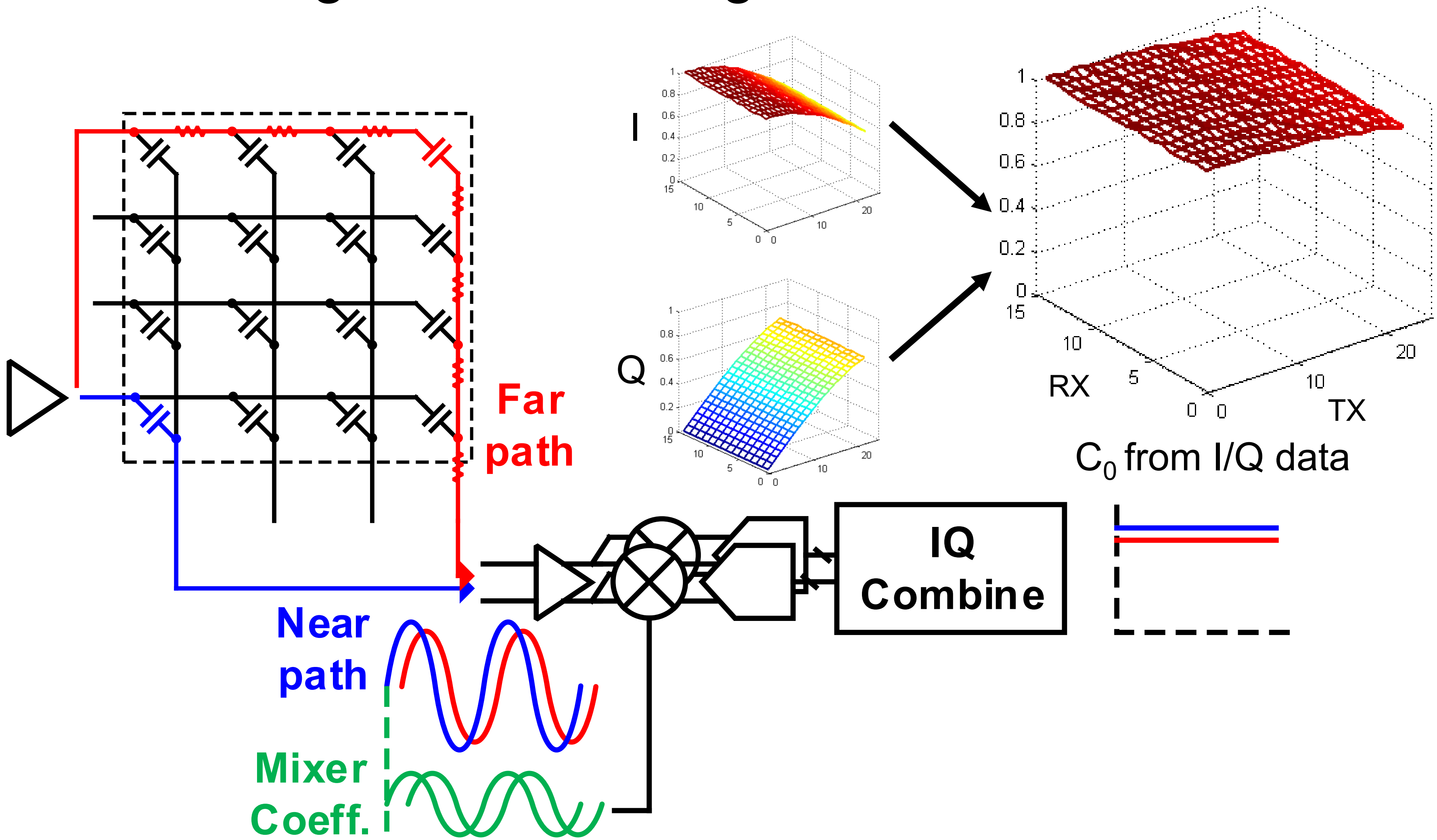




C_0 from I-data

Delay-loss Compensation

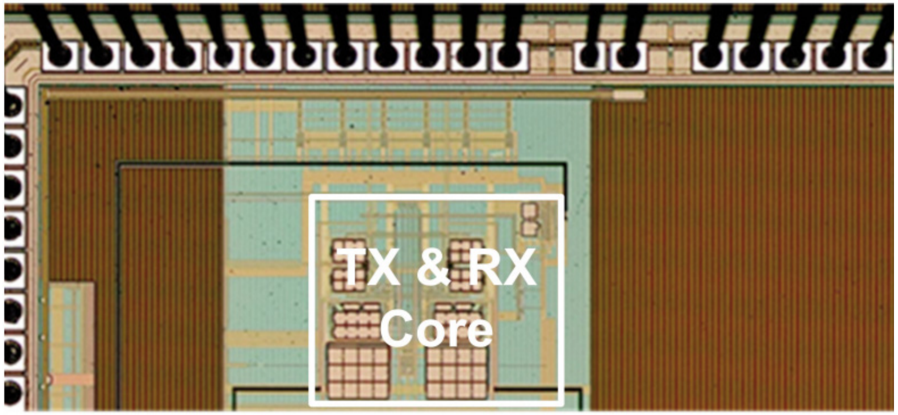
- I/Q mixing and combining catches full amplitude



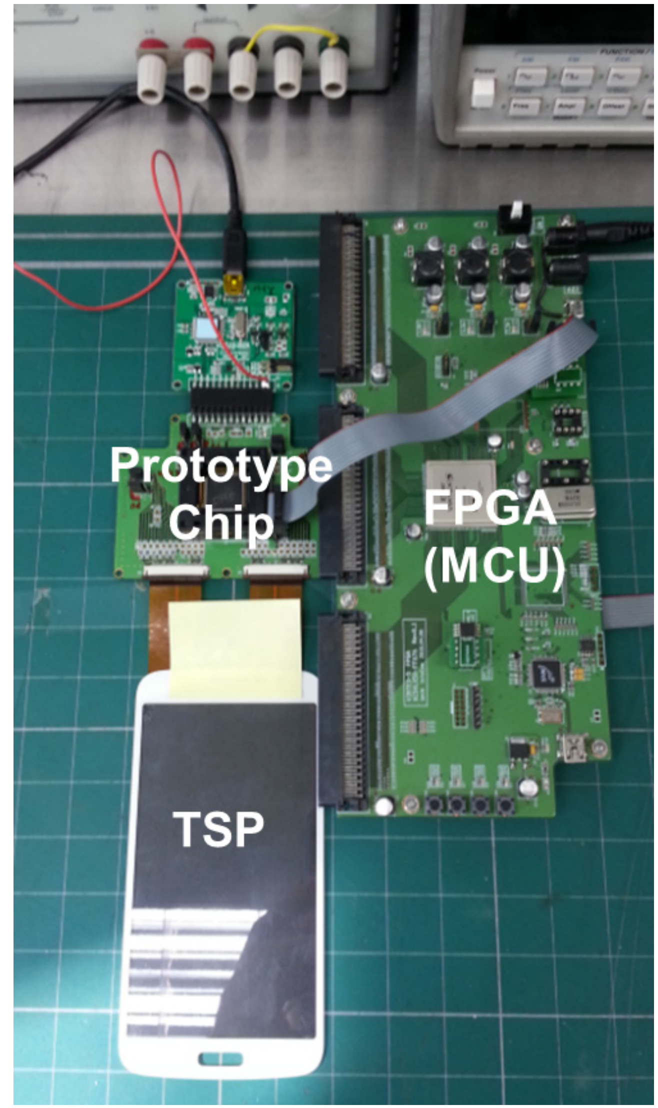
Outline

- Introduction & Motivation
- Coded-aperture-based Read-out
- Circuit Design Details
- Experimental Results
- Summary and Conclusion

Chip Implementation and Test

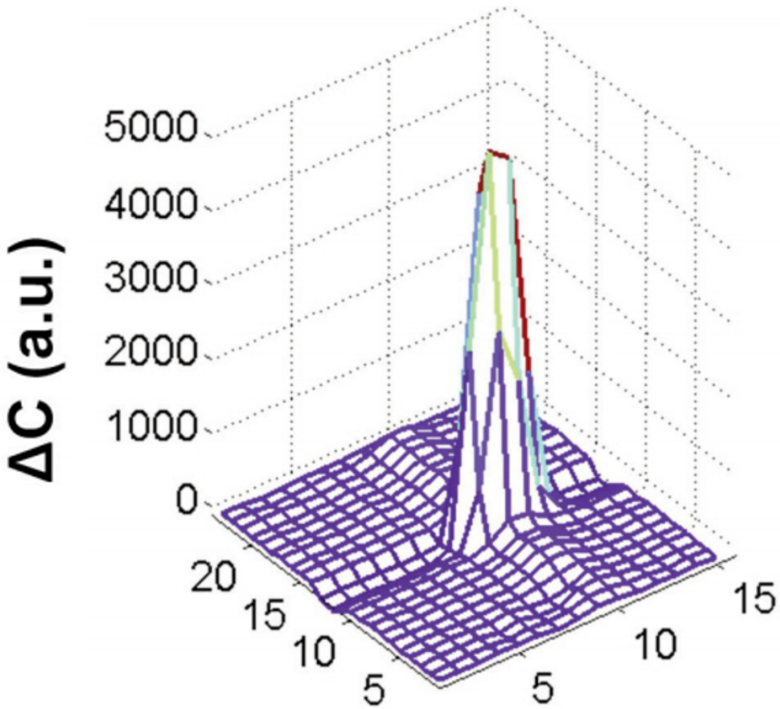


- 0.18um 1.8/3.3V TRs
- TX: 3.3V, RX: 3.3/1.8V
- Analog active area
  : 0.46 mm^2
- Analog power
  : 2.6 mW
- TSP for test
  : 24-TX $_X$ 16-RX

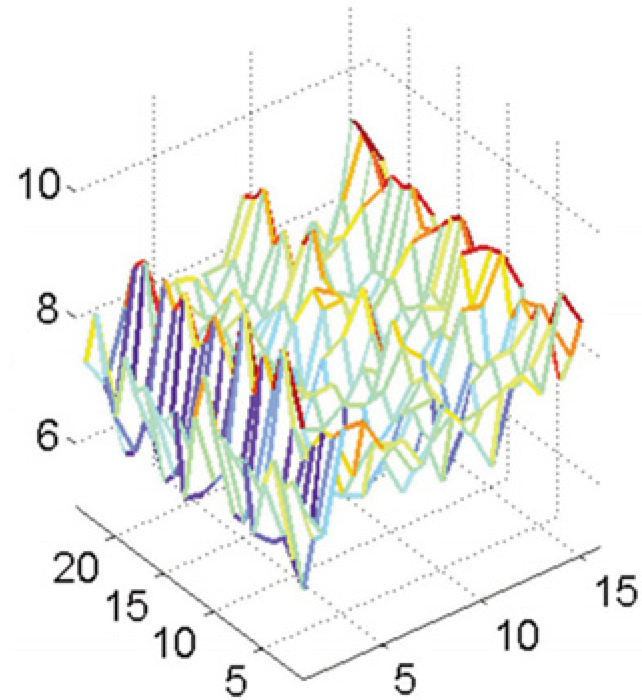


Measurement Results

- Reconstructed images



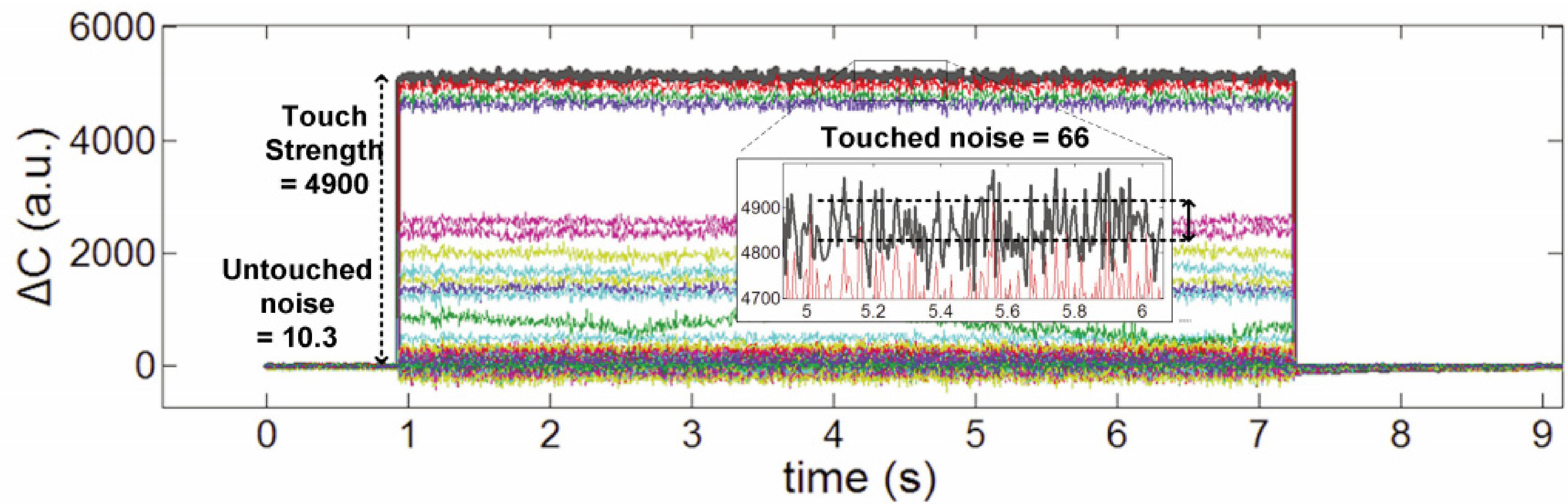
Finger response image



Untouched noise (100-frame rms)

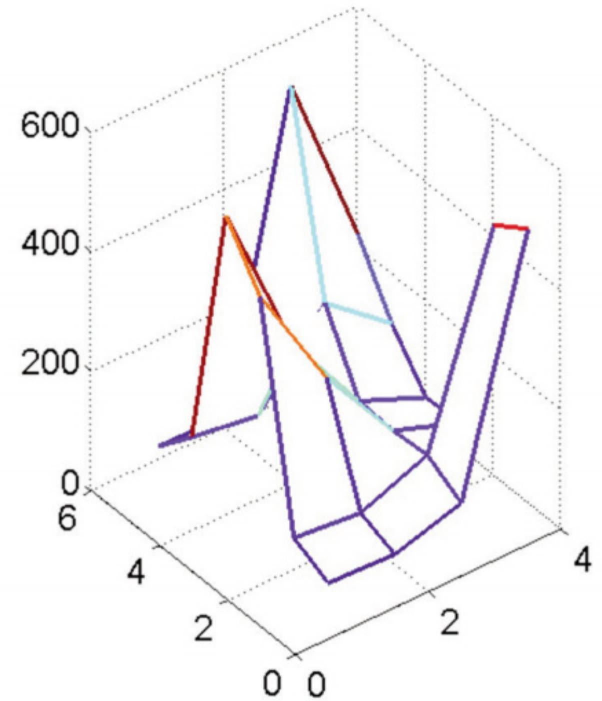
Measurement Results

- Recorded all-node data for finger
  - Untouched SNR (Touch strength / noise $\text{rms}_{\text{untouched}}$) ~ 53 dB
  - Touched SNR (Touch strength / noise $\text{rms}_{\text{touched}}$) ~ 38 dB

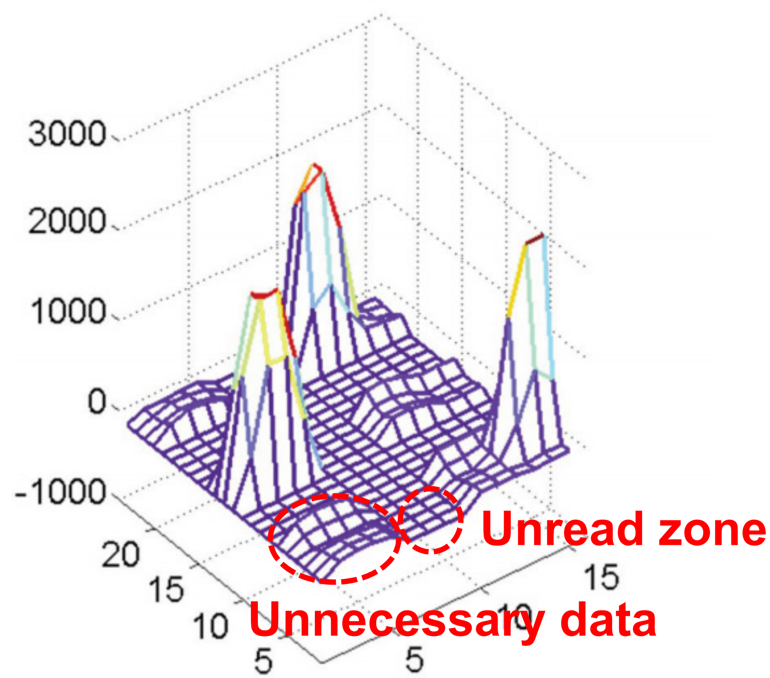


Measurement Results

- Reconstructed images
  - Resolution-scaling mode for faster frame-rate



Low-resolution image for 3-finger touch event



Local high-resolution image

Summary

- Enhancement on analog hardware optimization
- Maintaining high noise-immunity from [4]

	[3]	[4]	This Work
Process	0.35μm 3.3V CMOS	0.18μm 3.3/1.8V CMOS	0.18μm 3.3/1.8V CMOS
Channels (TX×RX)	27×43	30×24	24×16 (40 TRXs)
Scan rate	120Hz	240Hz	160Hz
SNR	39dB	55dB	53dB
Analog Power	18.7mW	20mW	2.6mW
Analog Area	10.4mm^2	7mm^2	0.46mm^2

Conclusion

- Coded-aperture-based mutual TSP controller is presented for
  - Analog hardware compactness
  - High noise-immunity
  - Suggesting an architectural approach for optimizing 2D passive sensor-array read-out

- A simple yet effective RX circuit for TSP read-out is shown

A 160nW 63.9fJ/Conversion-Step Capacitance-to-Digital Converter for Ultra-Low-Power Wireless Sensor Nodes

Hyunsoo Ha[1], Dennis Sylvester[2],
David Blaauw[2], and Jae-Yoon Sim[1]

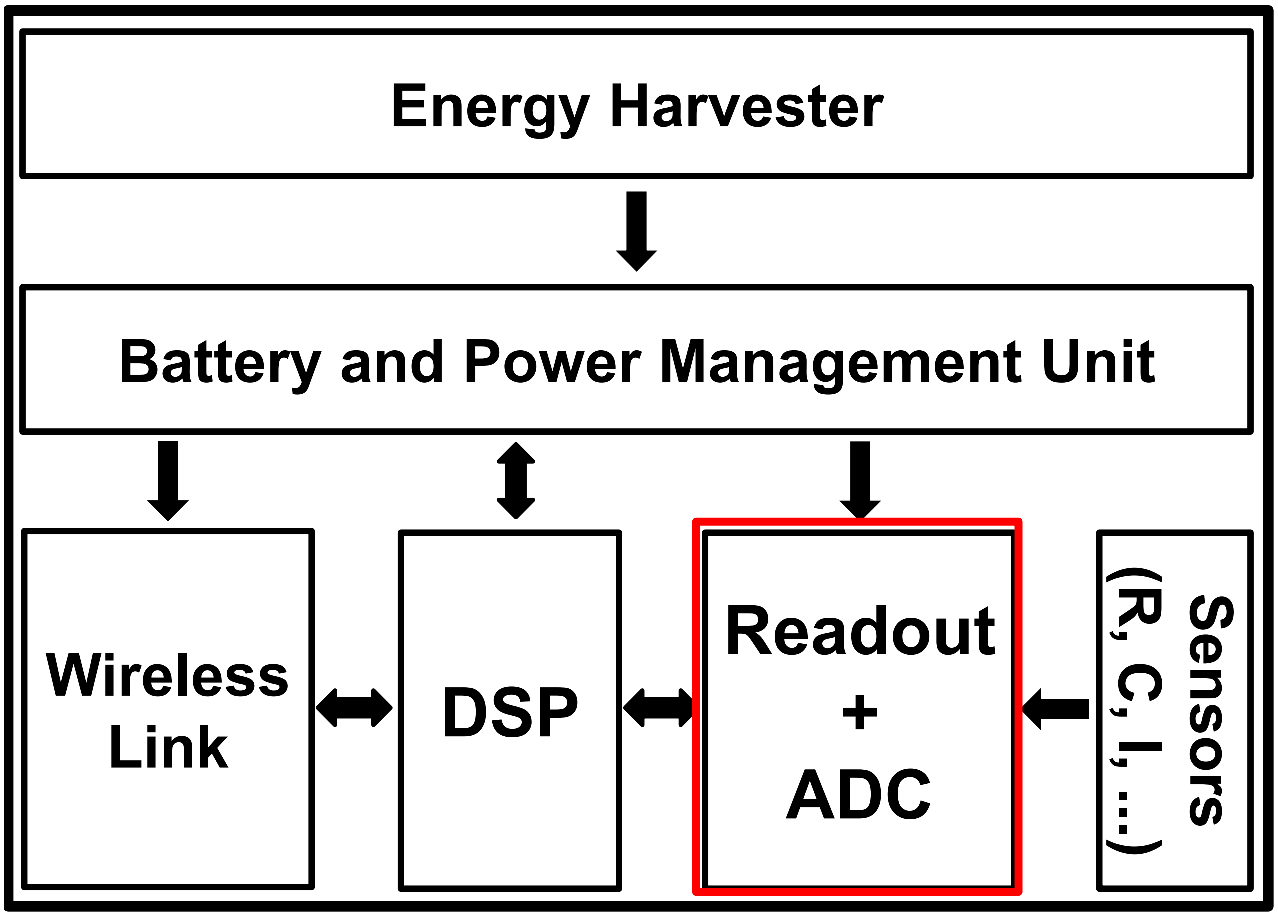
[1]POSTECH, Pohang, Korea
[2]University of Michigan, Ann Arbor, MI

Outline

- Introduction
  - Wireless Sensor Node
  - Previous Approaches for Capacitance Sensing
- Proposed Capacitance-to-Digital Converter
  - Correlated Double Sampling
  - Asynchronous SAR ADC
- Implementation Results
- Conclusion

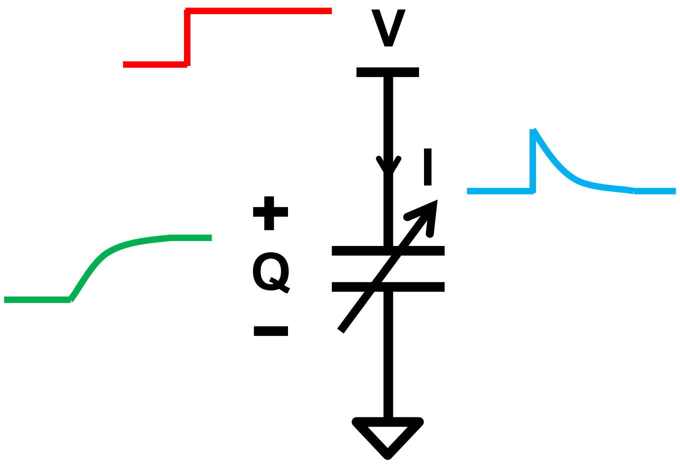
Wireless Sensor Node (WSN)

- Energy autonomous system to acquire and analyze data of surroundings through sensor



Capacitance Sensing

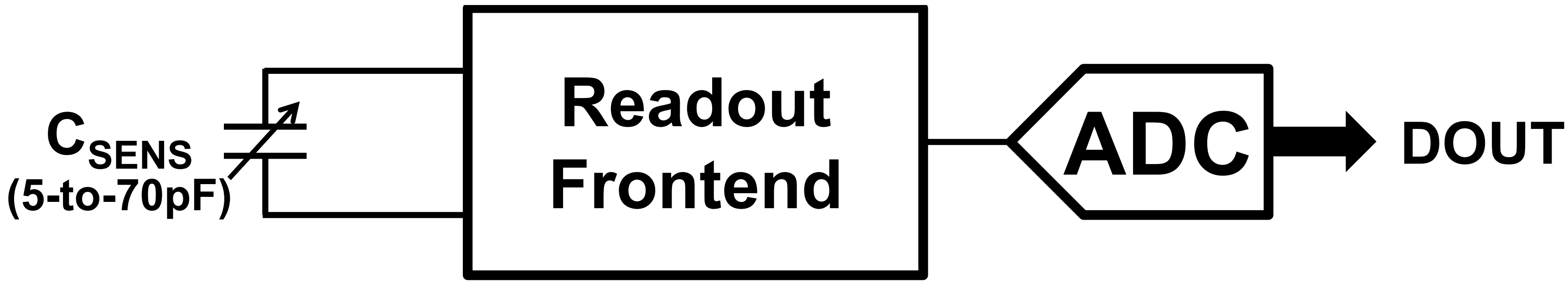
- Utilizes changes of capacitance according to variation of surroundings



- Zero static current during signal readout

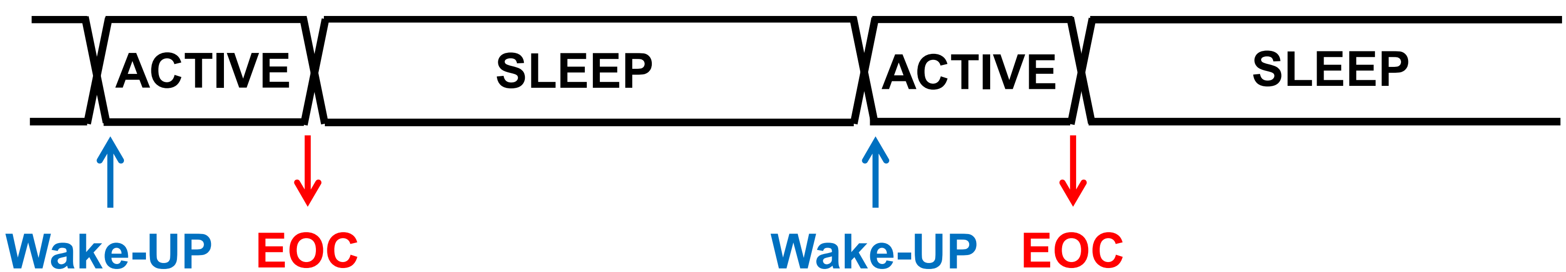
- Widely adopted in various sensing applications
  - Pressure
  - Displacement
  - Humidity

Requirements on CDC for WSN



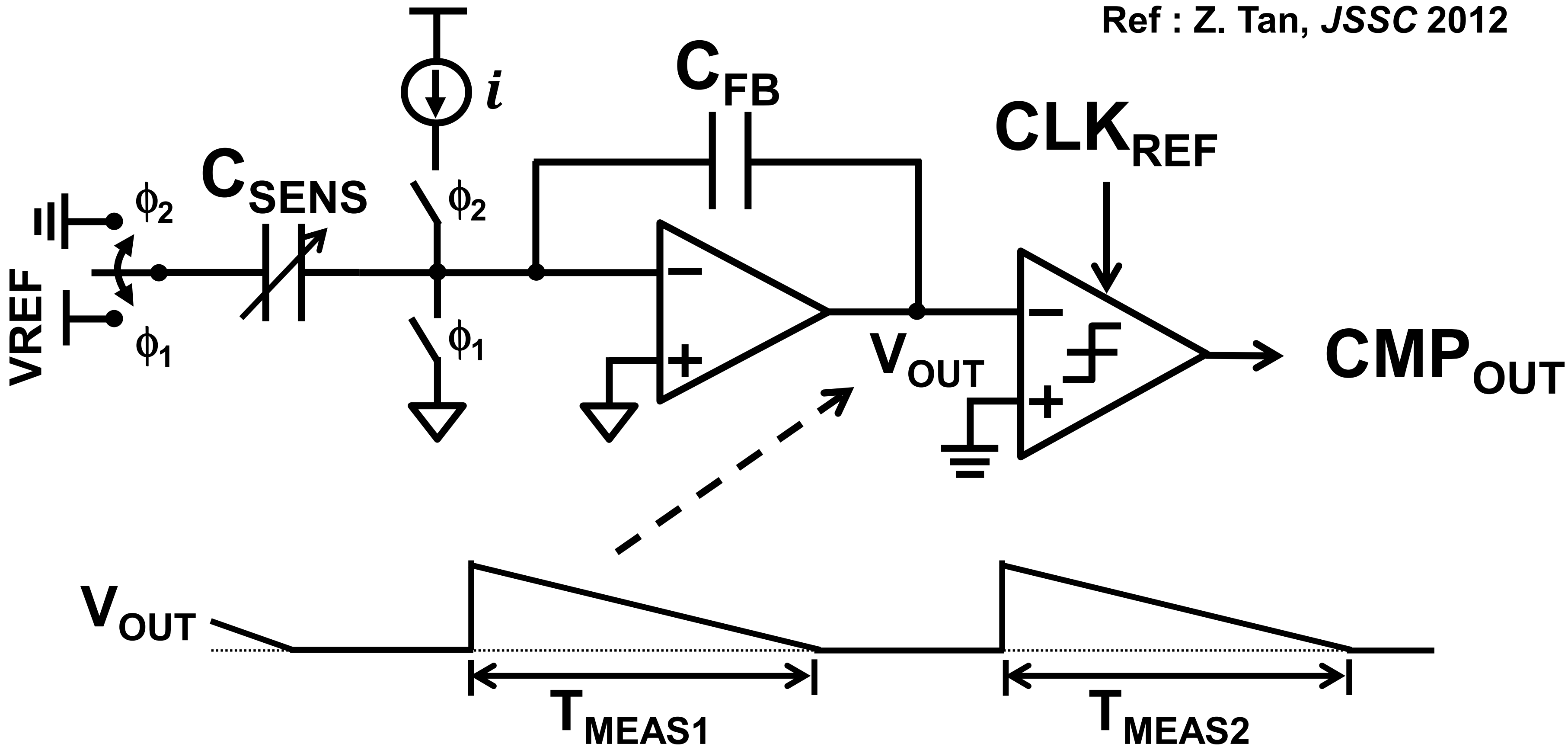
- Good energy efficiency
  - Ultra-low-power consumption with fine resolution
  - State-of-the-art FoM = 1.4pJ/conversion-step

- Support intermittent operation with fast wake-up



Previous Approach - PWM

Ref : Z. Tan, *JSSC* 2012

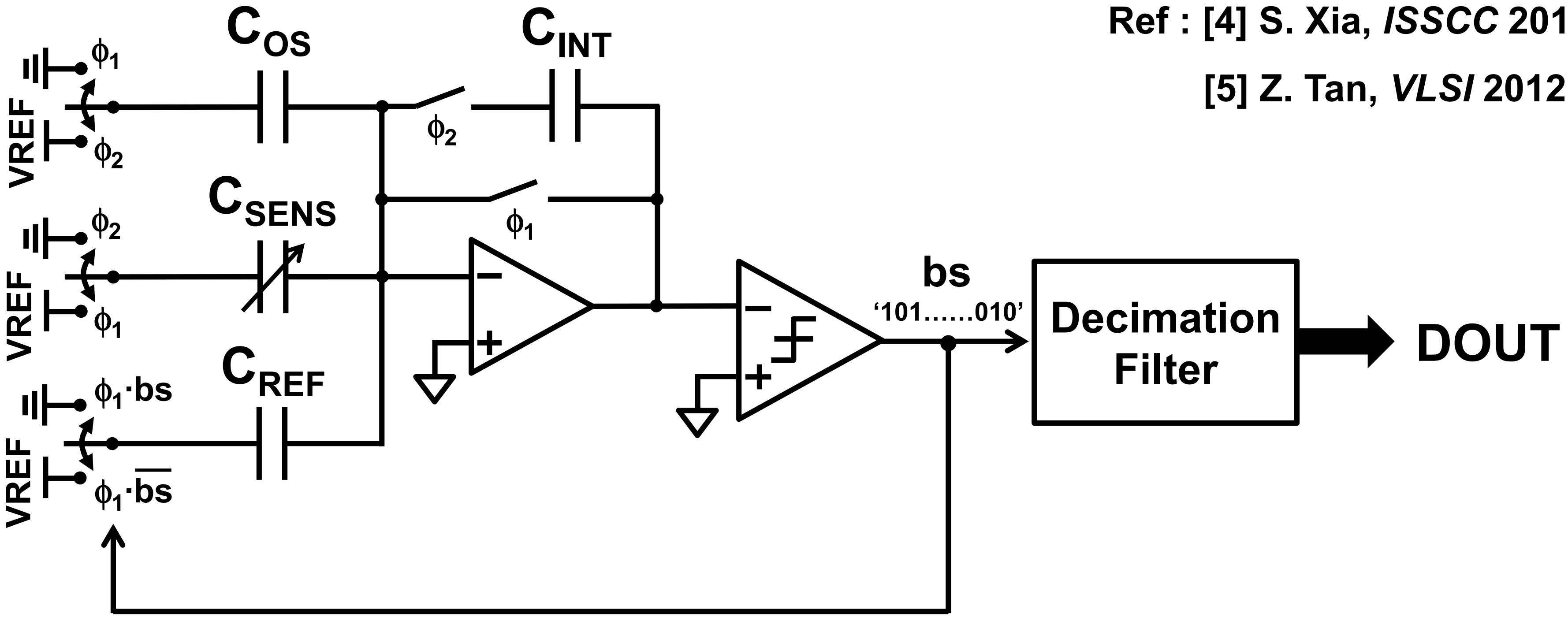


- **Good for intermittent operation**
- **Requires large number of CLK_{REF} cycles**

Previous Approach - ΔΣ Converter

Ref : [4] S. Xia, *ISSCC* 2012,

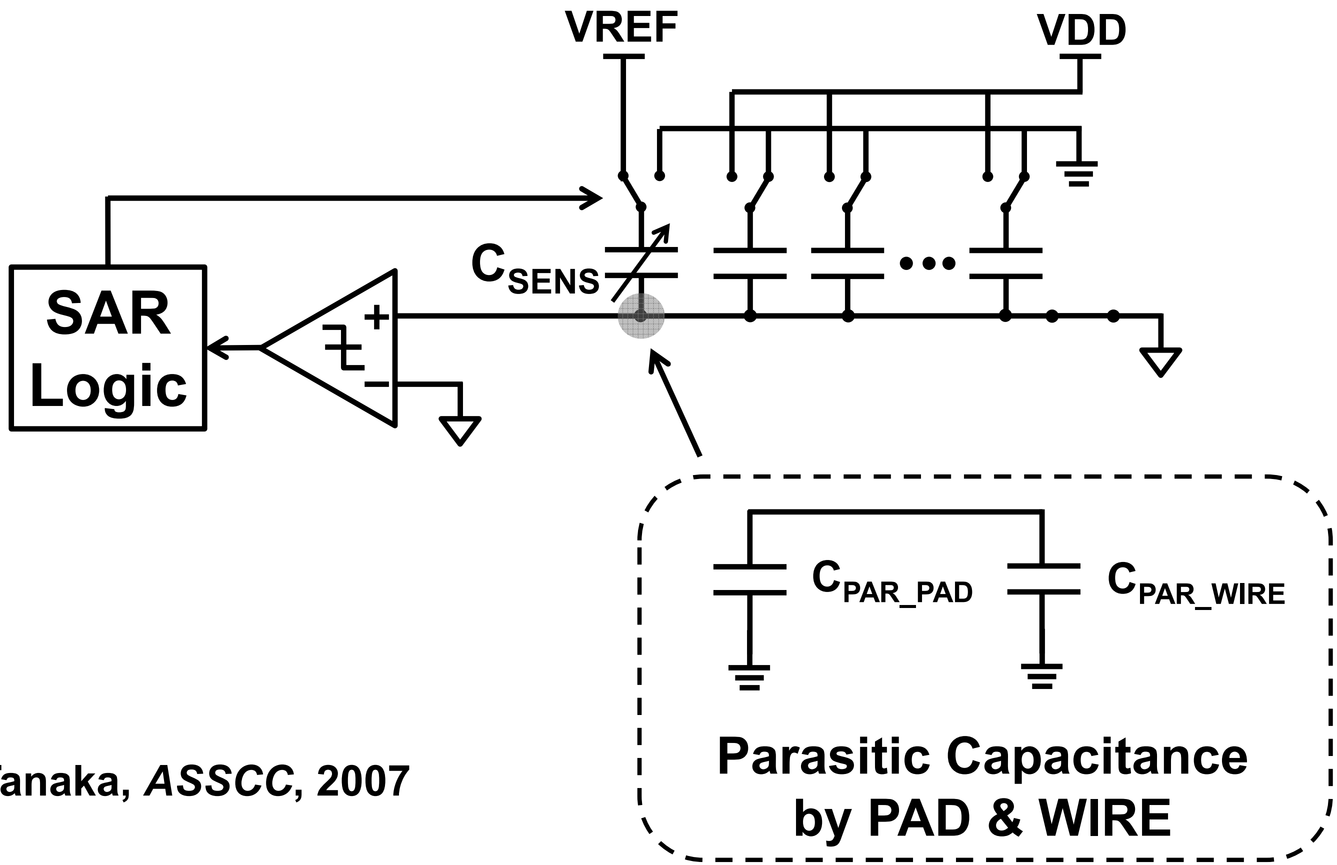
[5] Z. Tan, *VLSI* 2012



$$C_{SENS} - C_{OS} = \frac{\sum (bs \cdot C_{REF} - \overline{bs} \cdot C_{REF})}{N}$$

- **Fine resolution (<100aF)**
- **Numerous cycles to produce the 1st valid result**

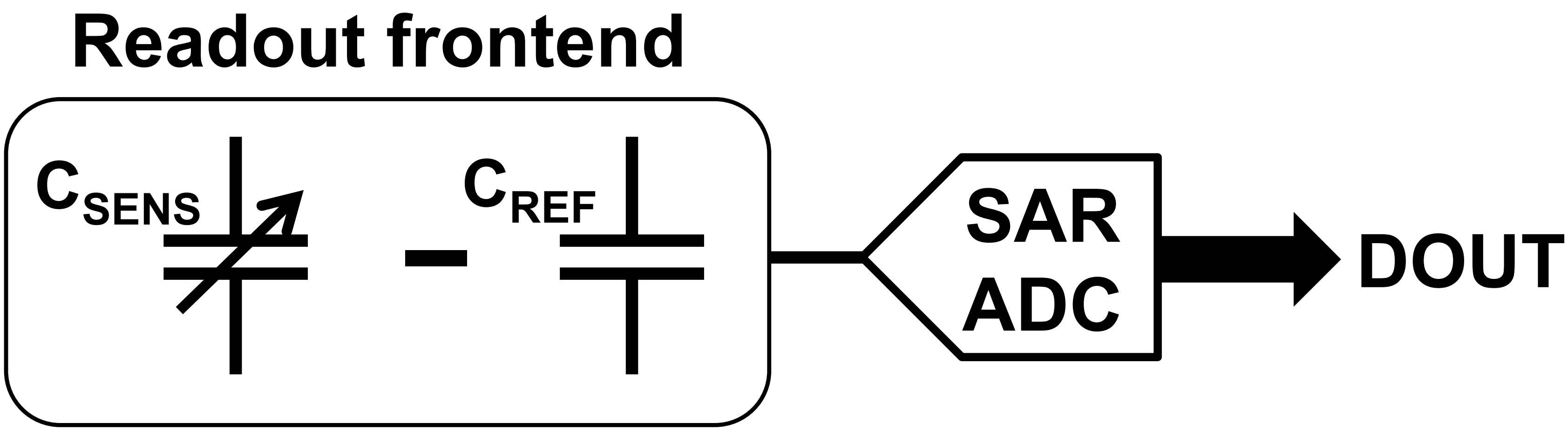
Previous Approach - SAR



Ref : [2] K. Tanaka, *ASSCC*, 2007

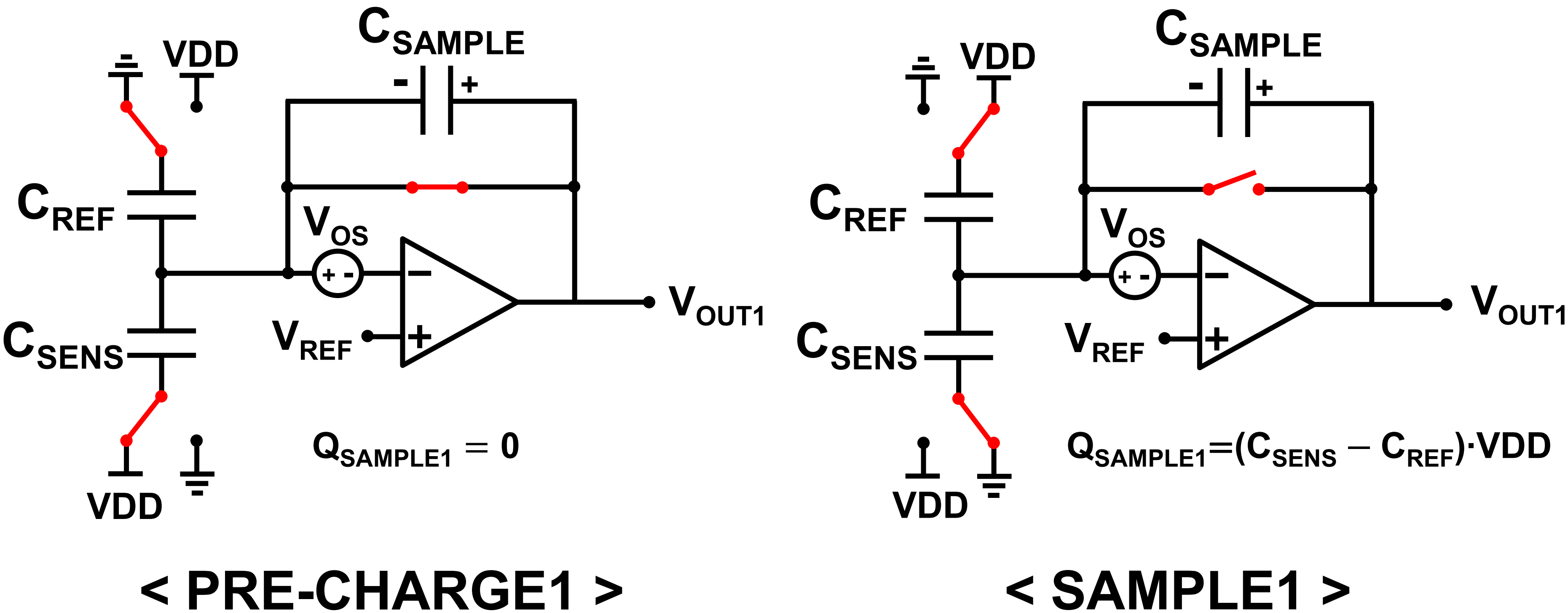
- **Good for intermittent operation & low-power**
- **Direct connection reduces signal amplitude**

Proposed CDC



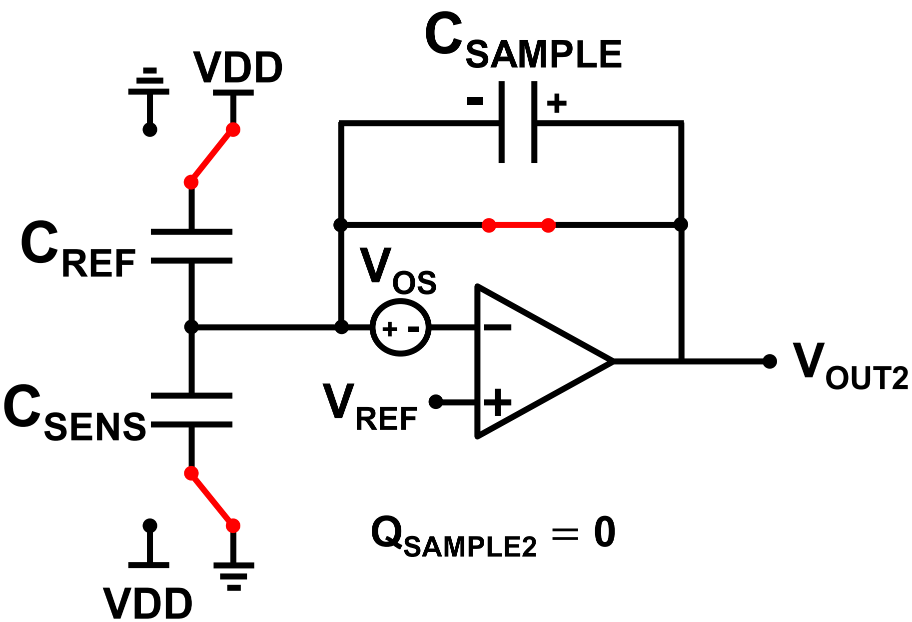
- **Difference sampling with CDS**
  - **Convert (C_{SENS} – C_{REF}) for fine resolution**
  - **Separation of C_{SENS} from the CDAC**
- **Sampling cap. for CDS reused in SAR ADC**
  - **Ultra-low-power consumption**
  - **Support intermittent operation**

CDS Procedure - 1

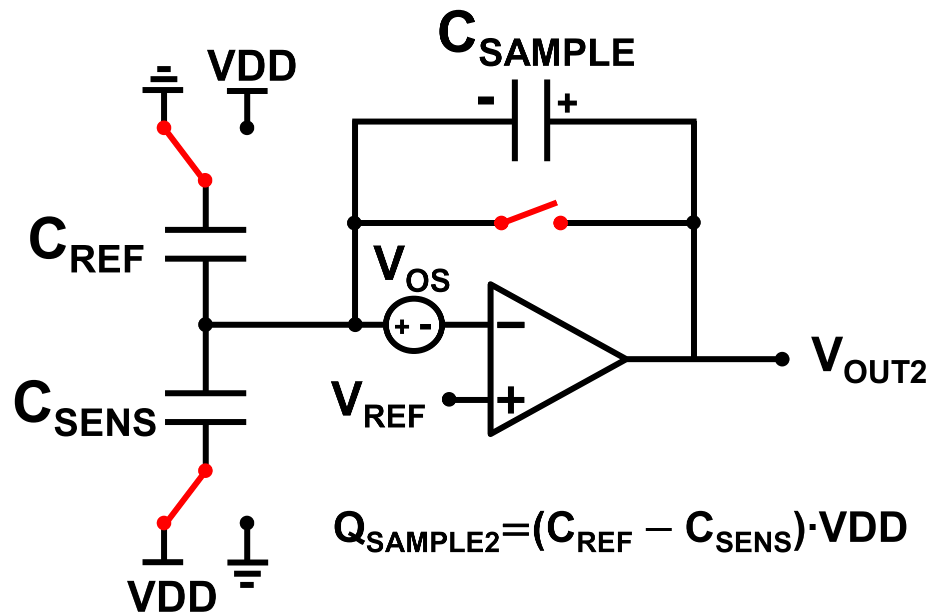


- **Charge proportional to ($C_{SENS} - C_{REF}$) stored in C_{SAMPLE}**
- **Q_{SAMPLE} not affected by V_{REF} and V_{OS} variations**

CDS Procedure - 2



< PRE-CHARGE2 >

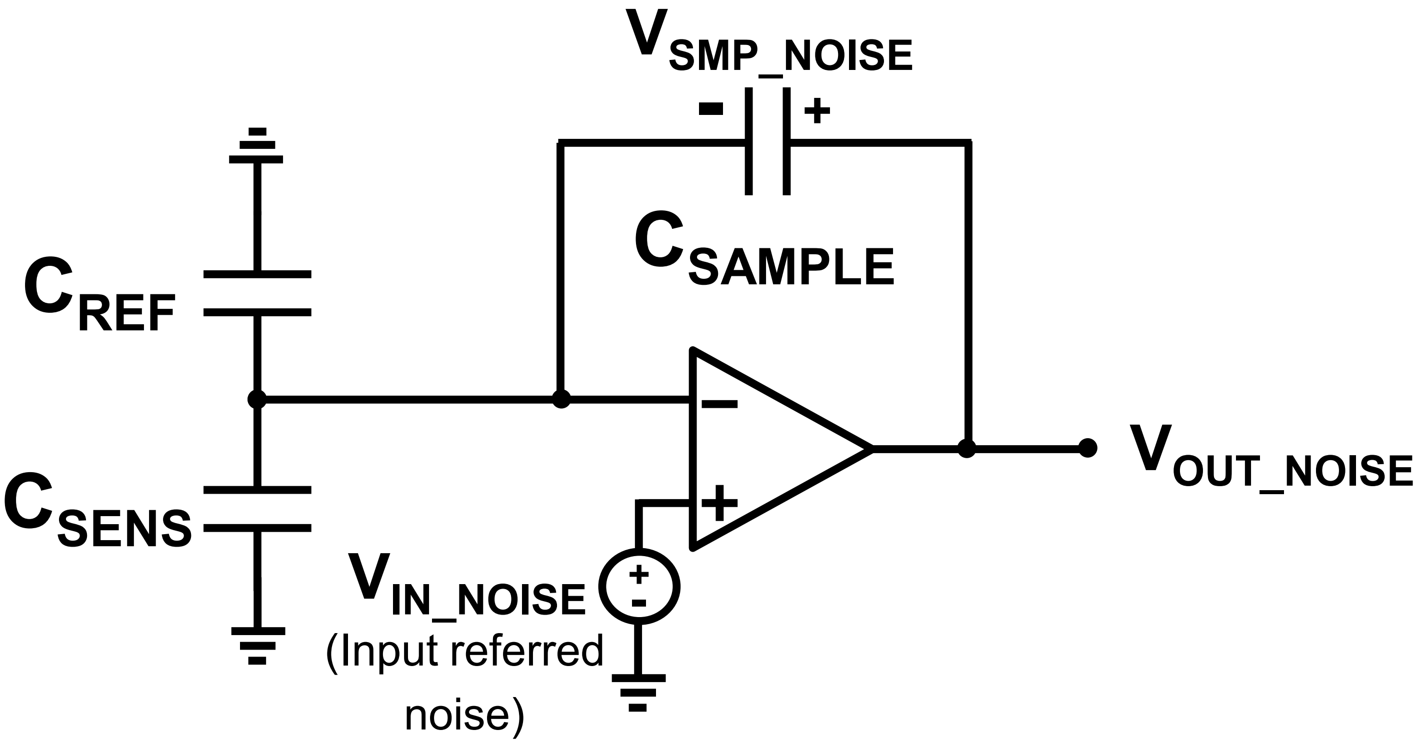


< SAMPLE2 >

$$Q_{SAMPLE} = Q_{SAMPLE1} - Q_{SAMPLE2} = 2\cdot(C_{SENS} - C_{REF})\cdot VDD$$

- Samples difference only with signal doubled

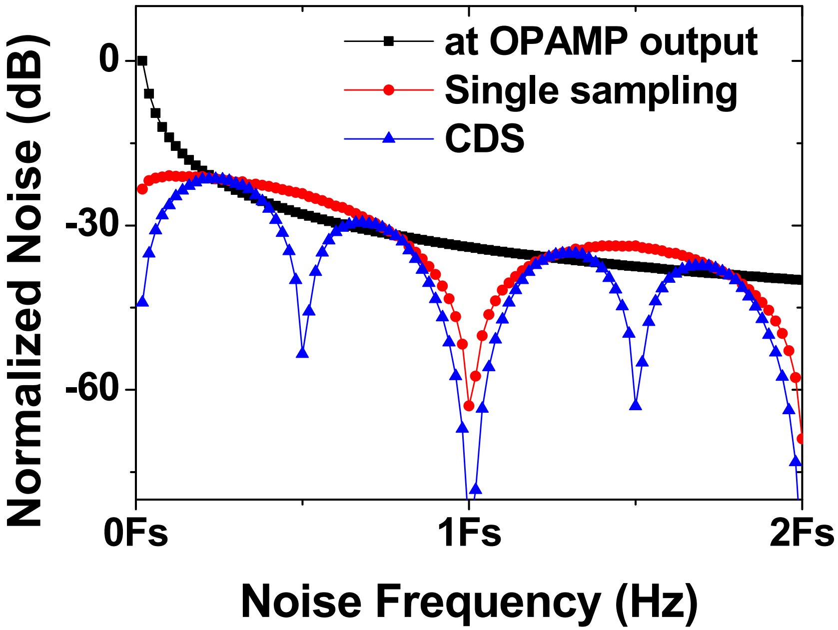
Effect of Noise : Noise Gain



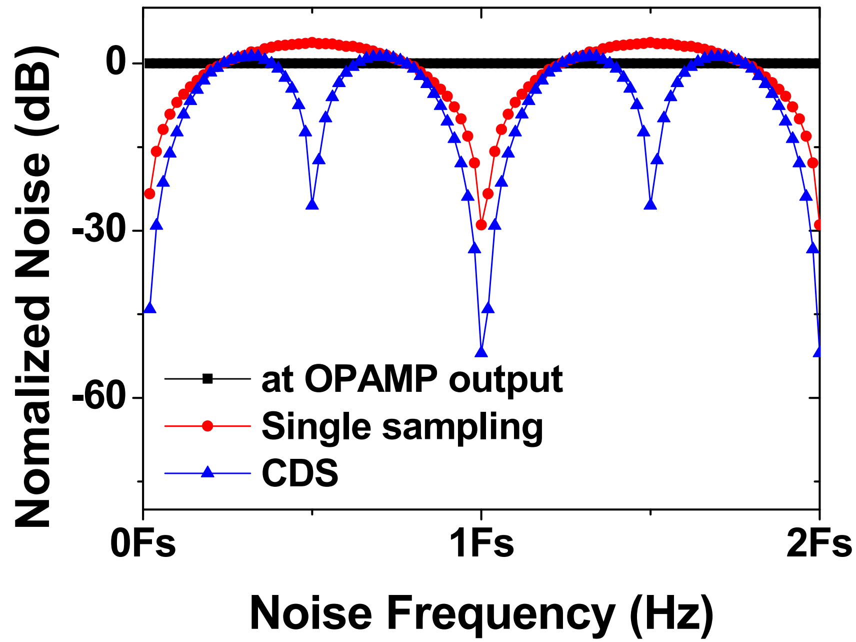
$$A_{SMP\_NOISE} = \frac{V_{OUT\_NOISE} - V_{IN\_NOISE}}{V_{IN\_NOISE}} = \frac{C_{REF} + C_{SENS}}{C_{SAMPLE}}$$

- **Larger C_{SENS} & C_{REF} cause more noise**

Simulated Noise



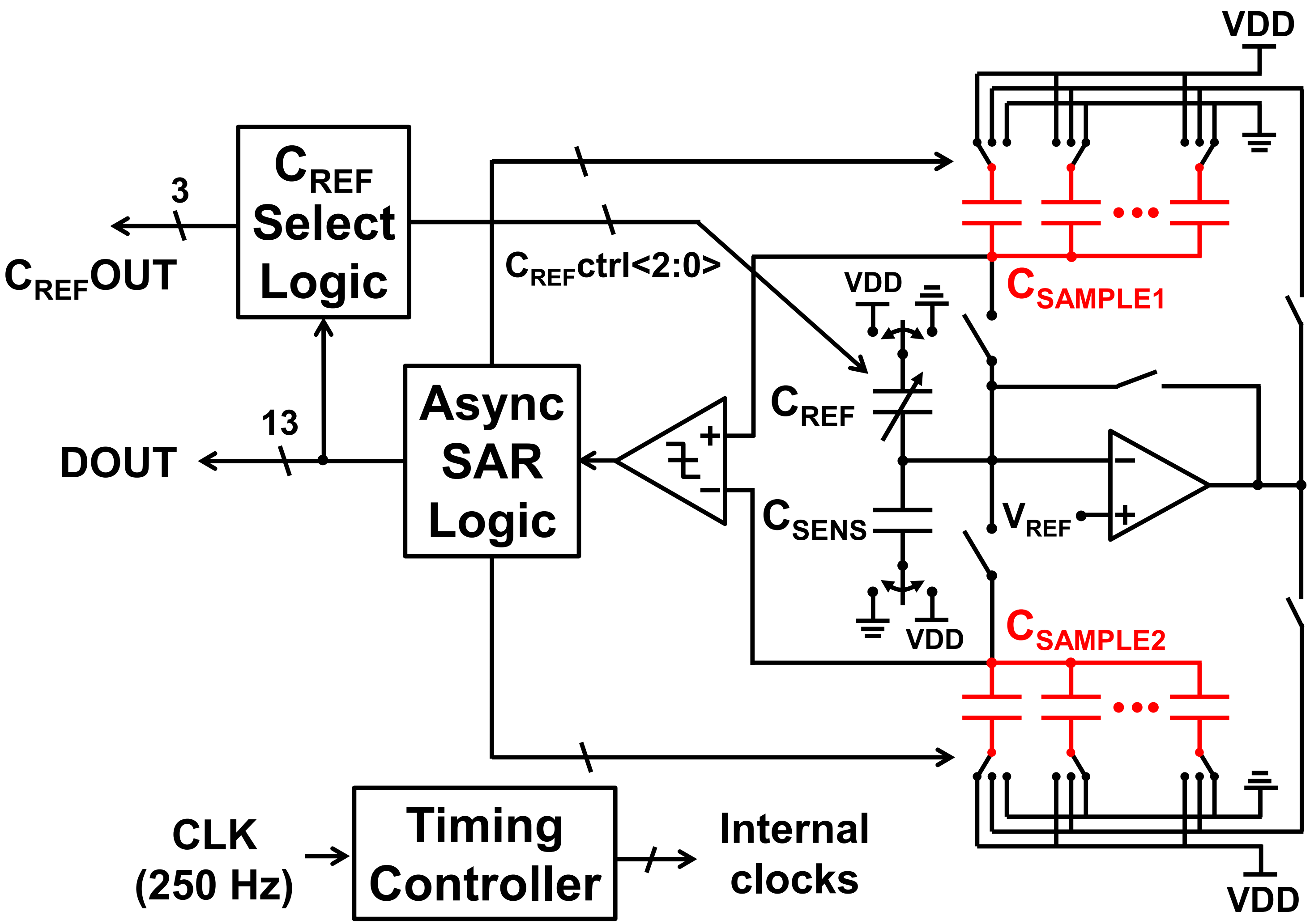
< Flicker noise >



< Thermal noise >

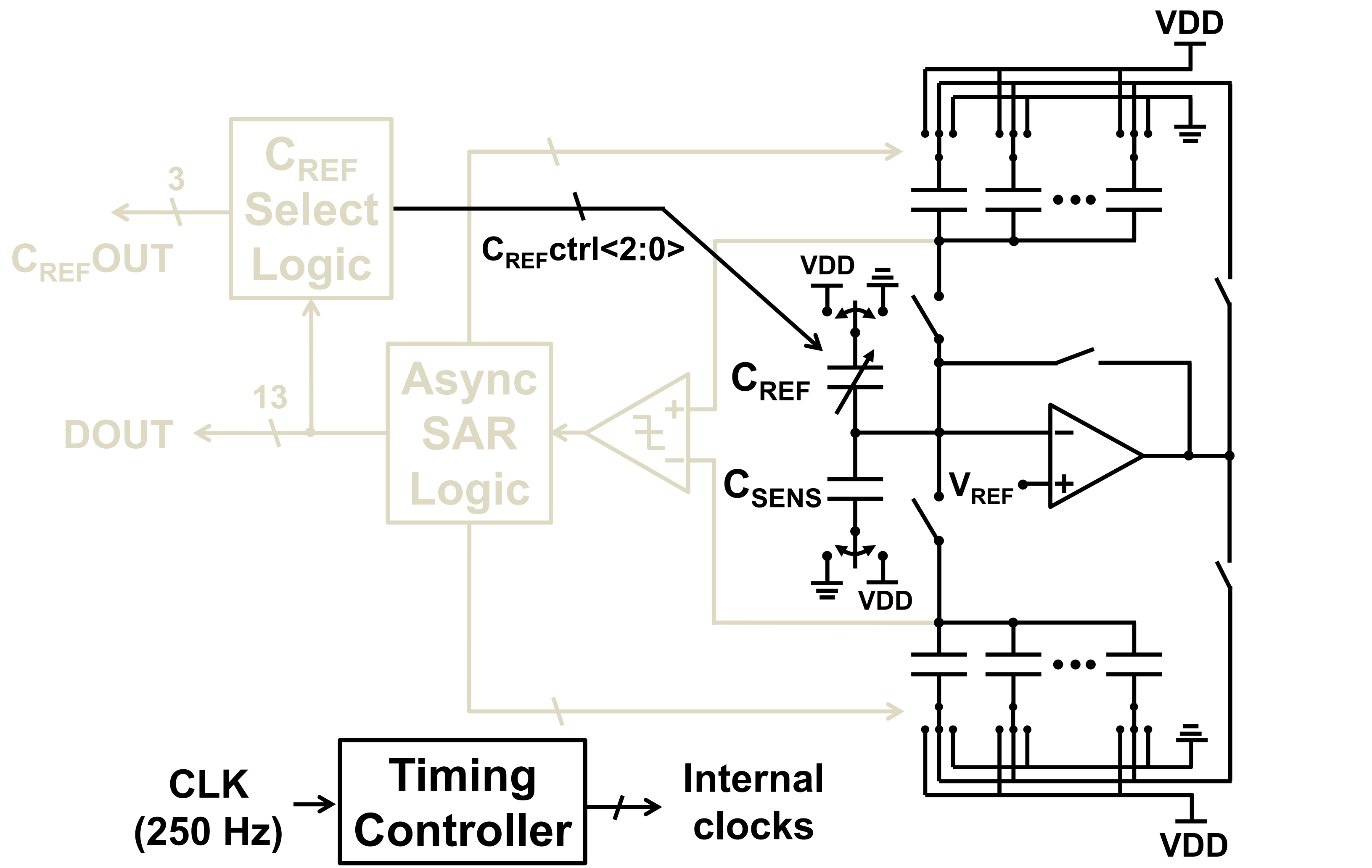
Noise (> 1Hz)	Single sampling	CDS
Flicker noise	- 2.3 dB	- 5.2 dB
Thermal noise	+ 0.5 dB	- 2.5 dB

C_{SAMPLE} Reused in SAR ADC



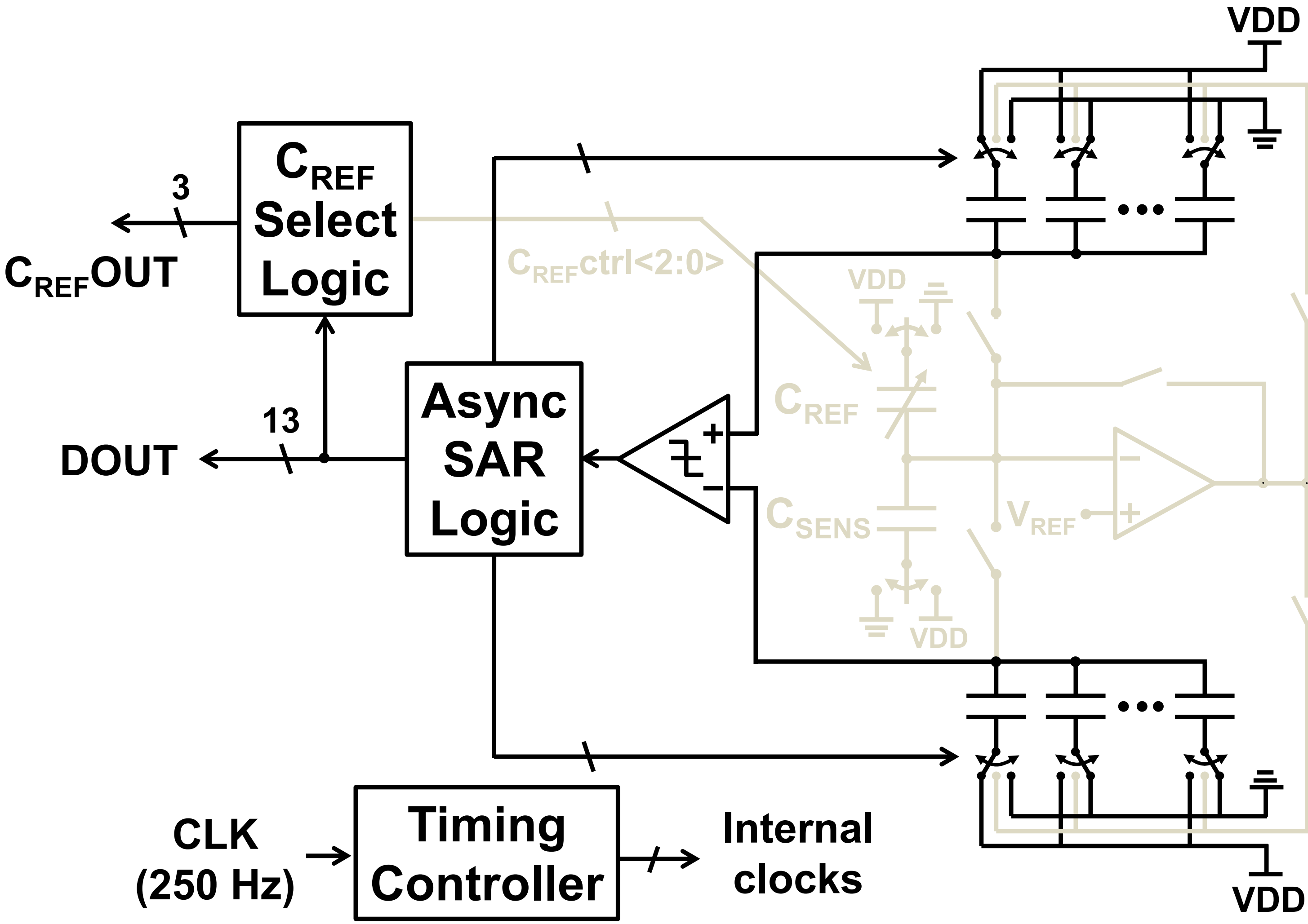
- **Saves charging power for ADC sampling**

Operation-1 : CDS on CDACs



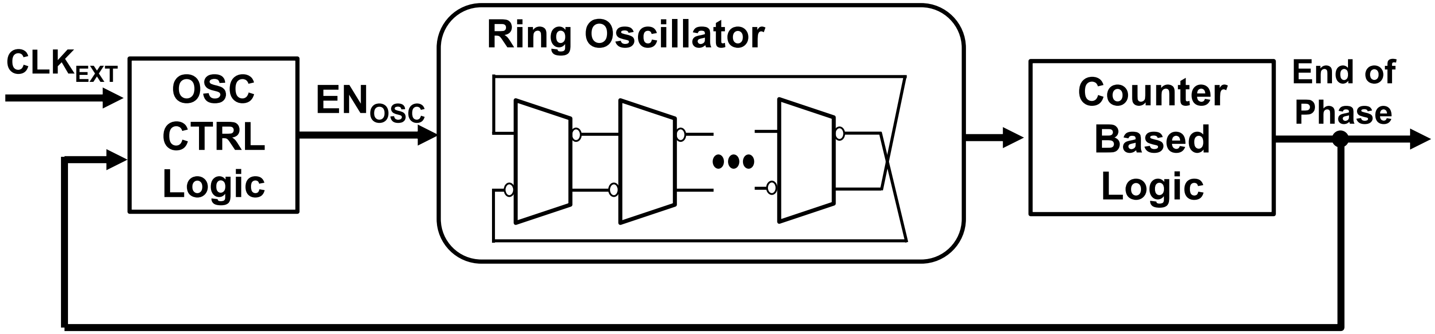
- **Differential output stored on CDACs**

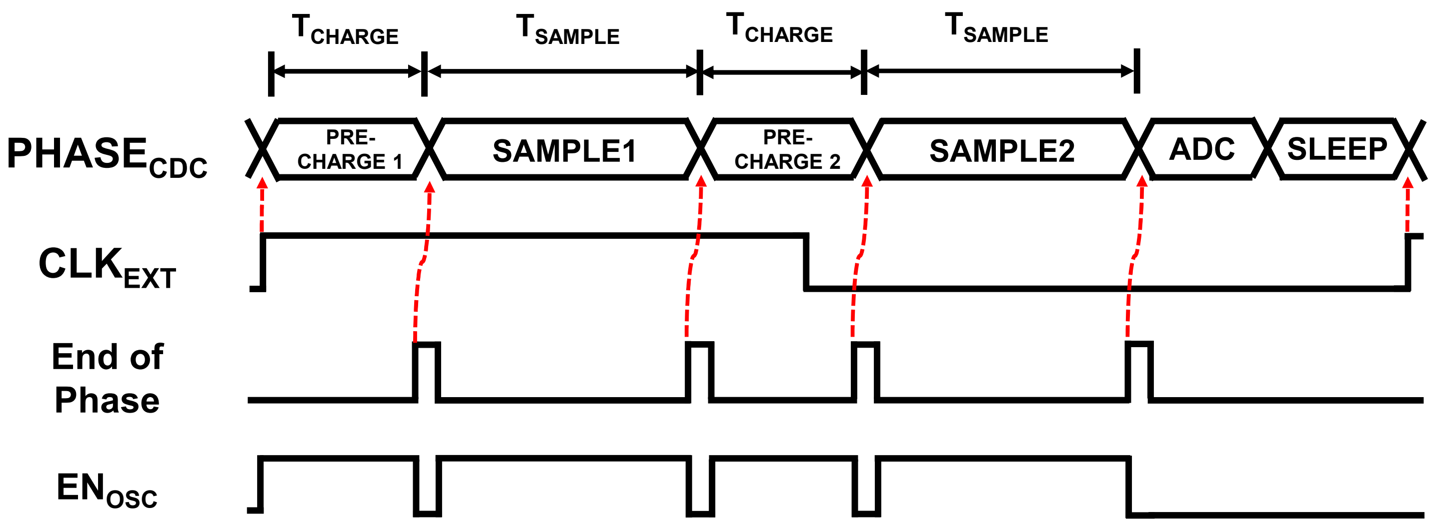
Operation-2 :A-to-D Conversion



- **Converting sampled result to 13b digital code**

Timing Control

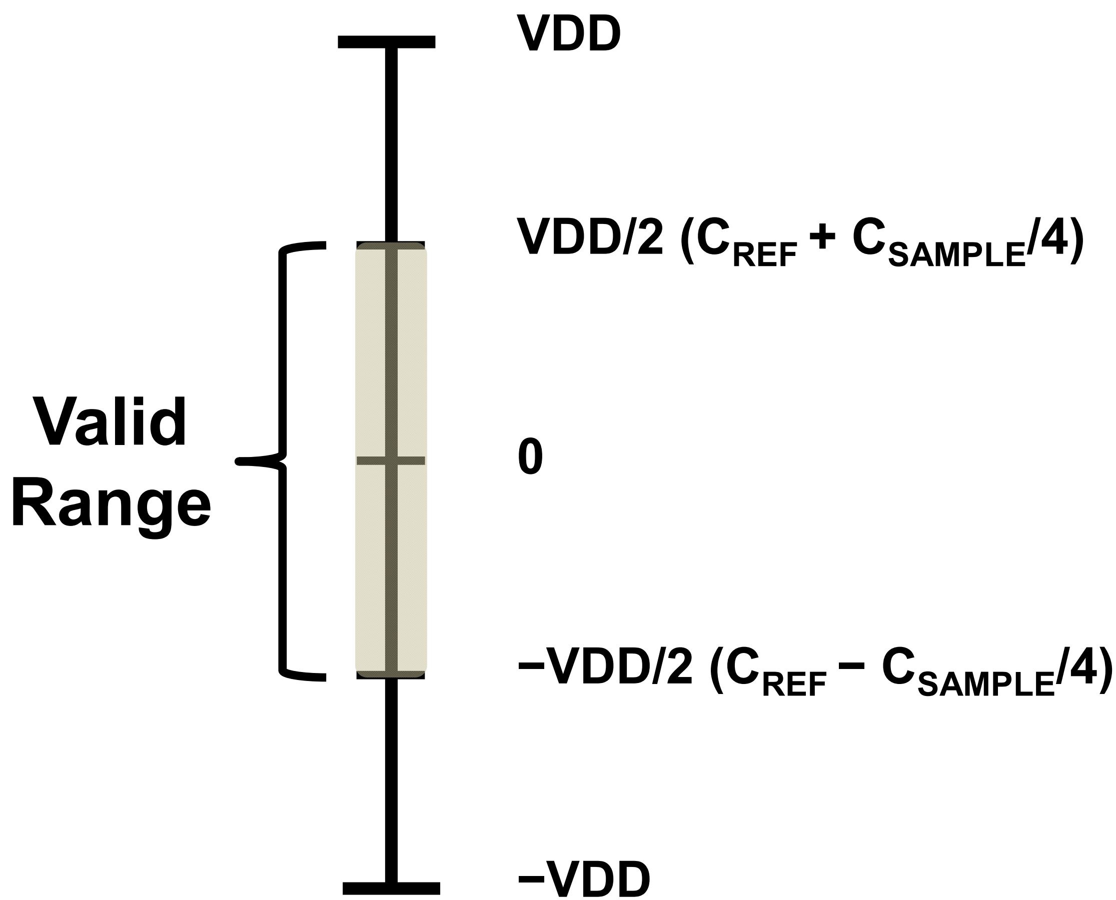




- Each transition of CLK$_{EXT}$ generates all control signals.
- Asynchronous SAR

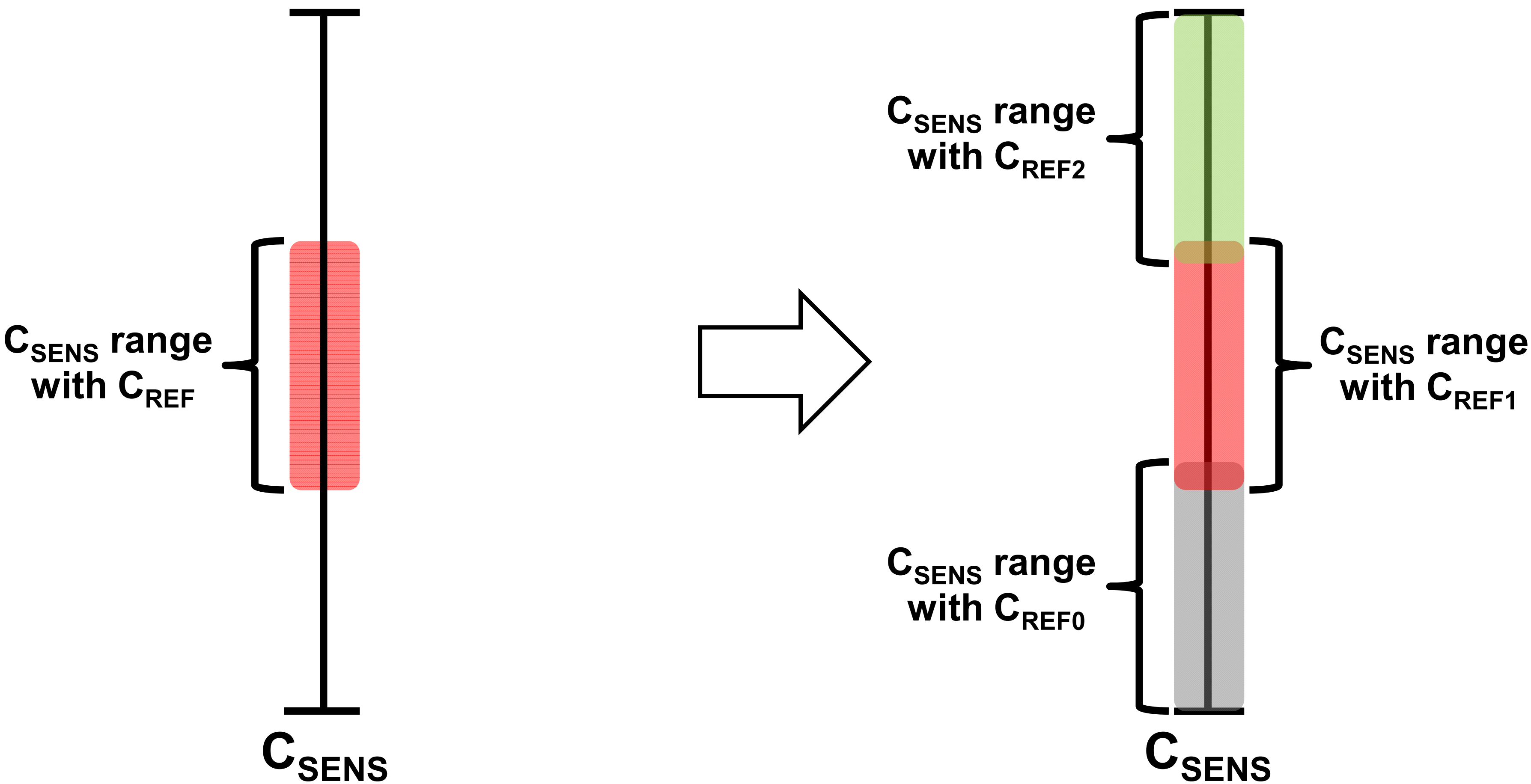
Set Valid Output Range of Amp

- **Output swing of amplifier limited**
  - → Amp output [-VDD/2 ~ VDD/2] is considered to be valid.



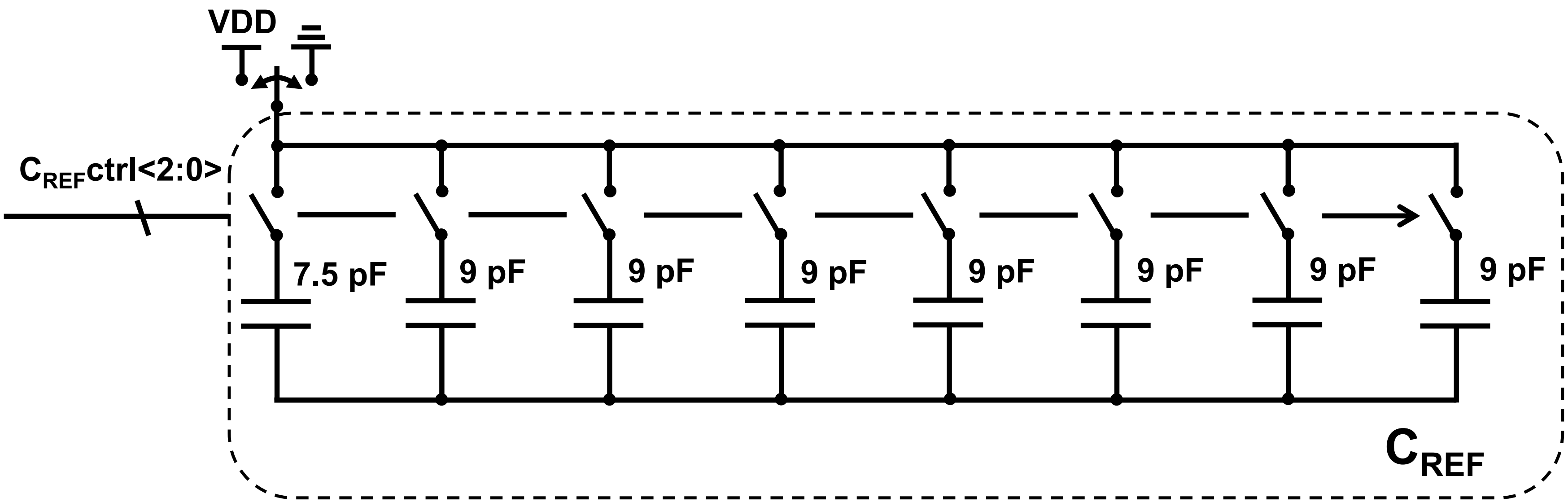
Conversion Range Extension

- **Extension of valid conversion range with multiple C_{REF}s**

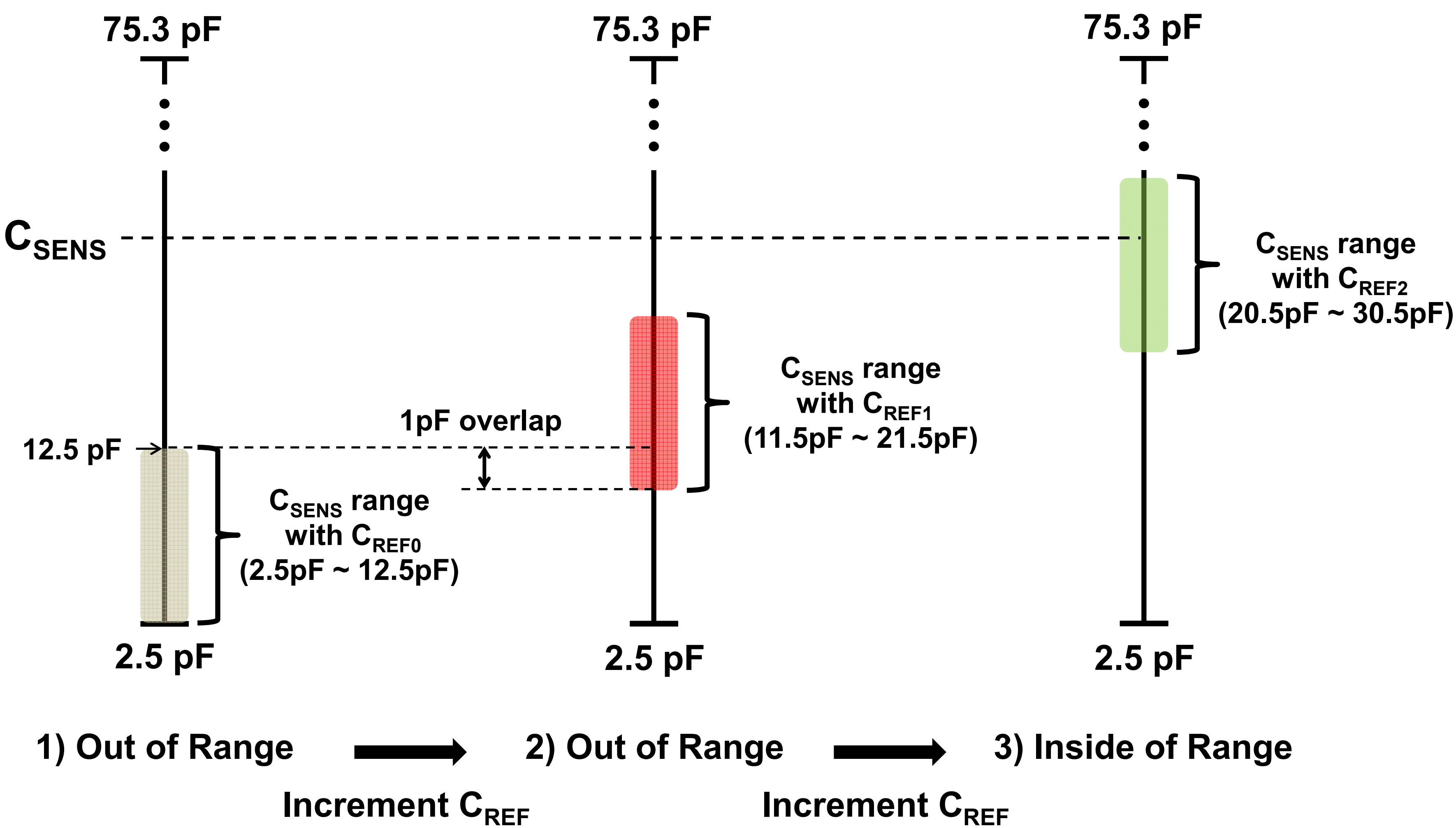


C_{REF} Array

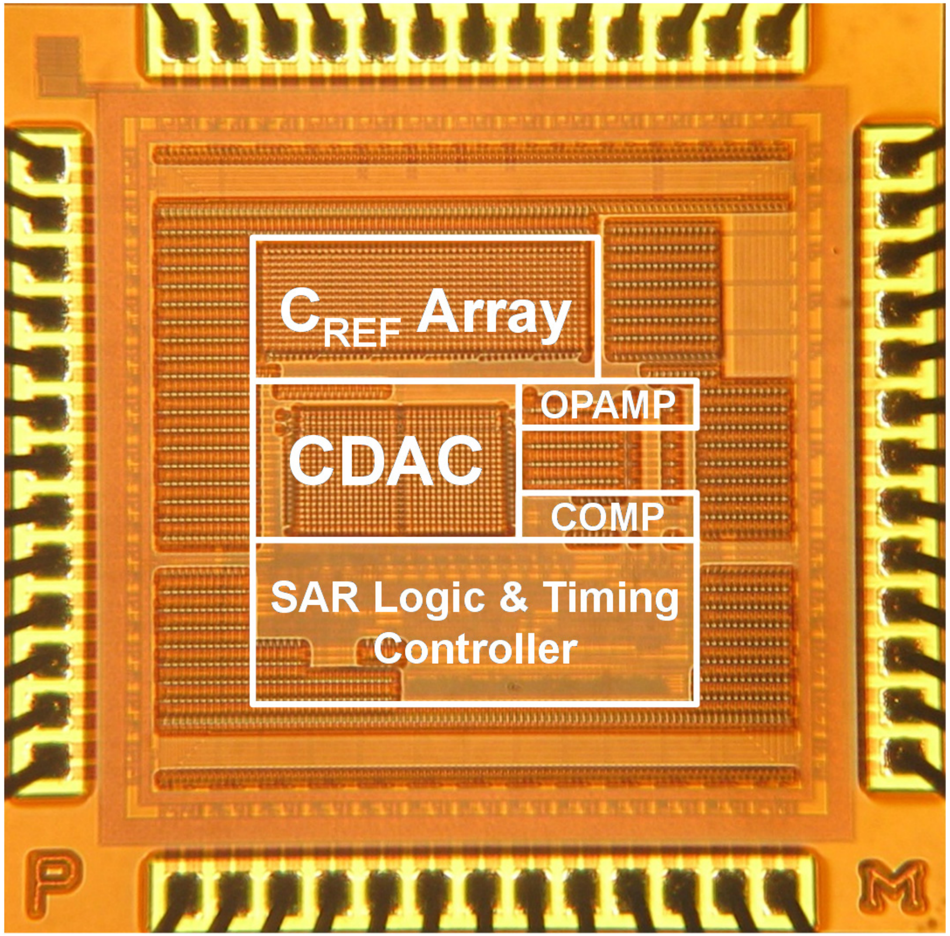
- **7.5-to-70.5pF in 9pF steps(8 C_{REF}s)**



C_{REF} Selection Procedure



Microphotograph

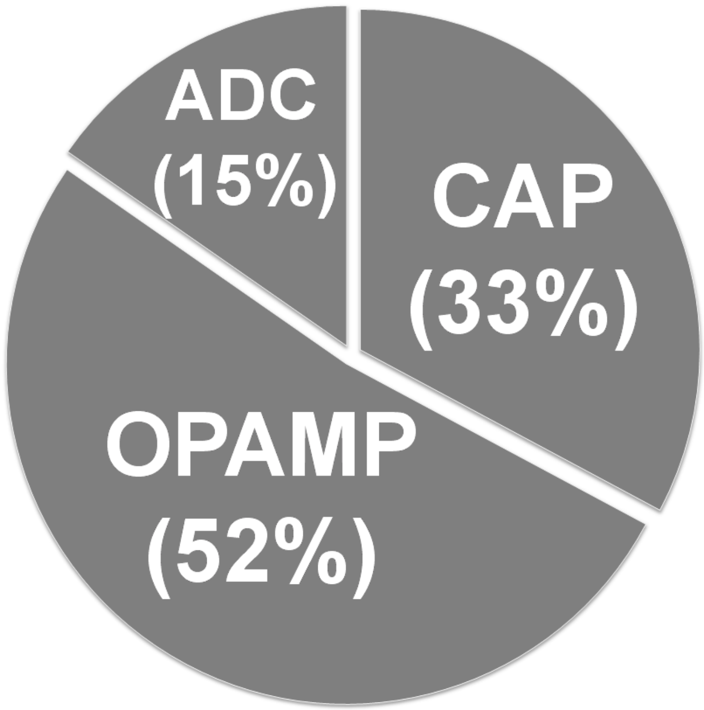


- **TSMC 180nm CMOS**
- **0.7 X 0.7 mm^2**

Measurements (@250 Sample/s)

C_{REF}	C_{SENS} range	Power
7.5 pF	2.5 ~ 12.5 pF	119 nW
16.5 pF	11.5 ~ 21.5 pF	127 nW
25.5 pF	20.5 ~ 30.5 pF	133 nW
34.5 pF	29.5 ~ 39.5 pF	139 nW
43.5 pF	38.5 ~ 48.5 pF	144 nW
52.5 pF	47.5 ~ 57.5 pF	148 nW
61.4 pF	56.4 ~ 66.4 pF	157 nW
70.3 pF	65.3 ~ 75.3 pF	160 nW

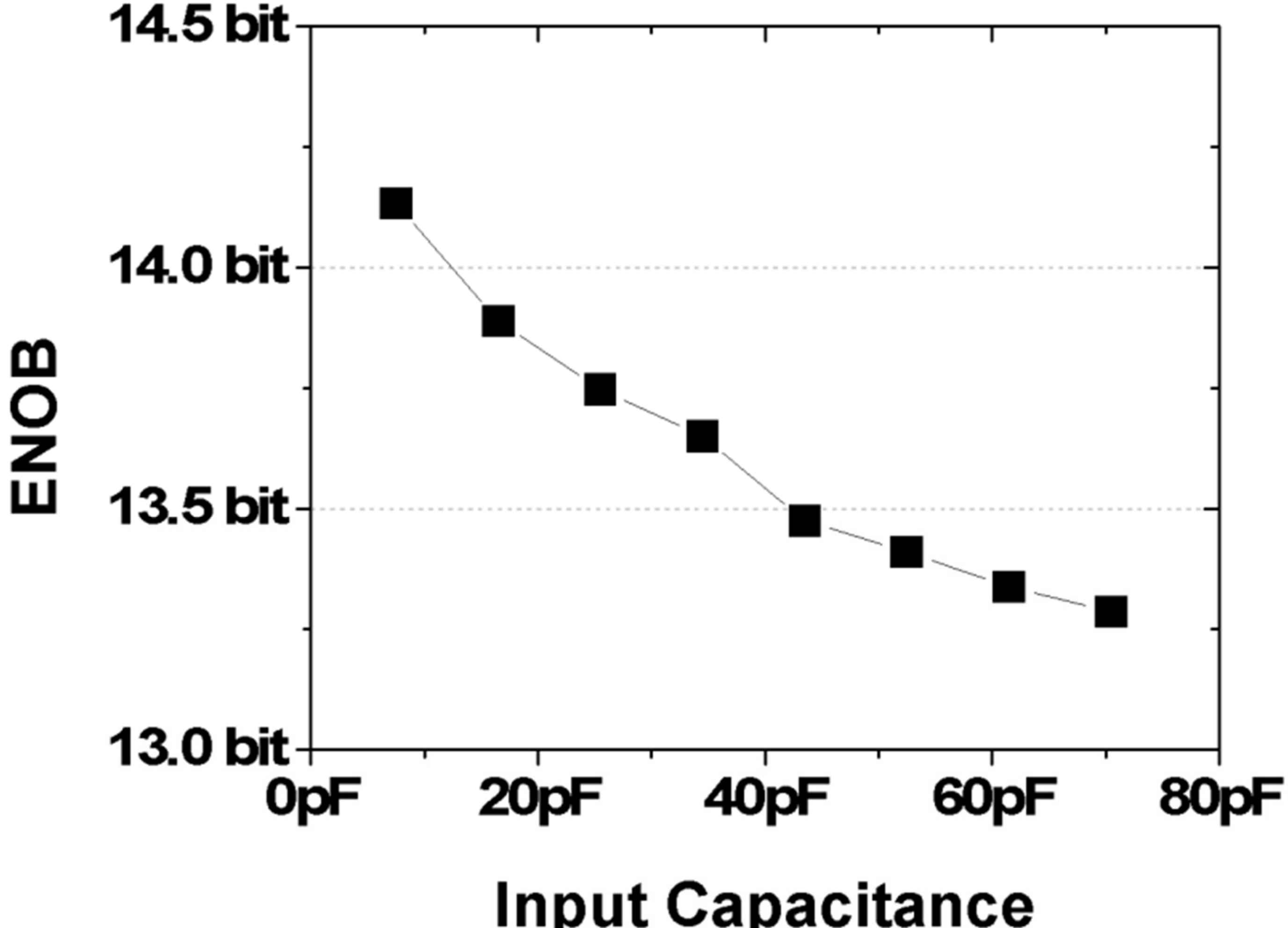
Power Breakdown



Block	Power
OPAMP	83 nW
CAP	52 nW
ADC	25 nW
Total	160 nW

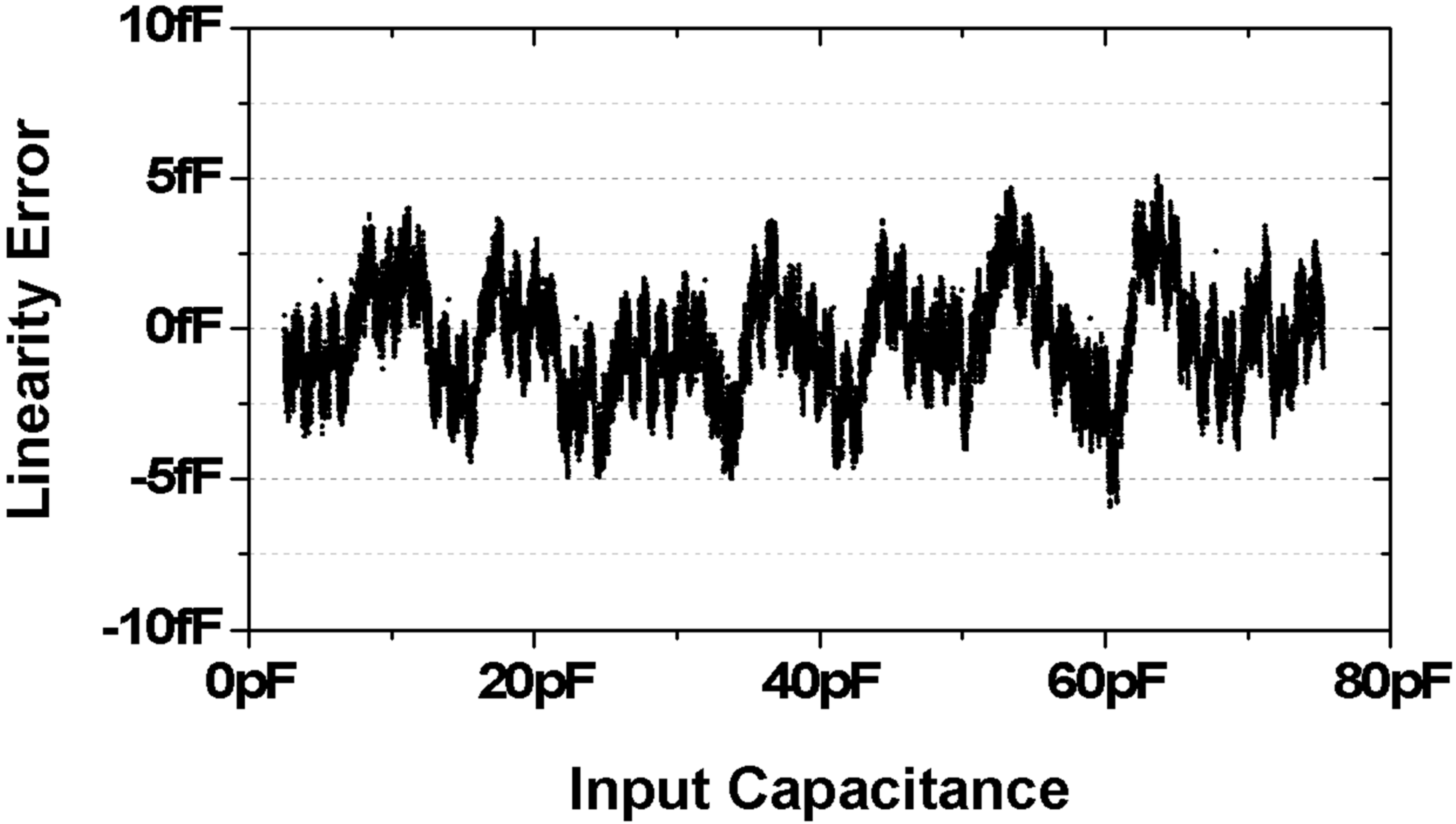
- **Energy/conv = 0.64 nJ/conv @ 250 Sample/sec**

Effective Number of Bits (ENOB)



ENOB = $(20 \times \log_{10}(Range/Resolution) - 1.76)/6.02$

Linearity Error



- **Error < 5.9 fF without missing code**

Performance Comparison

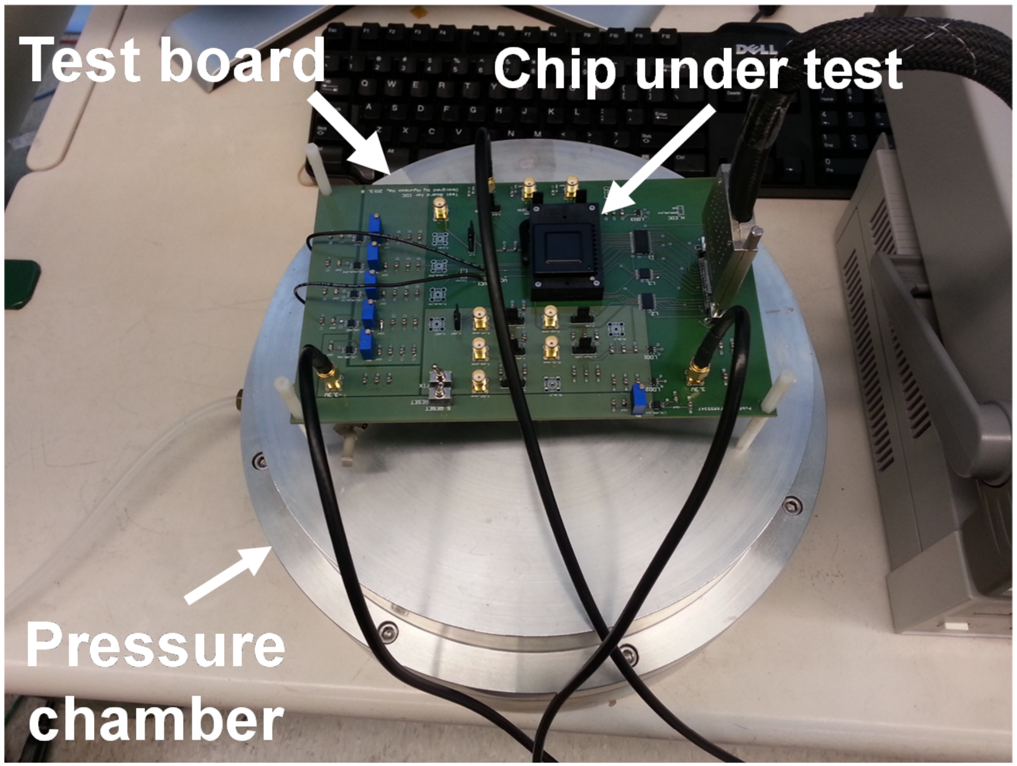
	[2] ASSCC 07	[3] ESSCIRC 11	[5] ISSCC 12	[6] VLSI 12	**This work**
Technology	0.18 μm	0.13 μm	0.35 μm	0.16 μm	**0.18 μm**
Conversion Method	SAR ADC	PLL-Based Conversion	ΔΣ modulation	ΔΣ modulation	**SAR ADC**
Supply	1.4 V	0.3 V	3.3 V	1.2 ~ 1.8 V	**1.2 V(Analog) 0.9 V(Digital)**
Input range	N/A	6.3 ~ 6.6 pF	8.4 ~ 11.6 pF	0.54 ~ 1.06 pF	**2.5 ~ 75.3 pF**
Meas time(ms)	0.004	1	0.02	0.8	**4**
Power	0.24 mW	270 nW	14.9 mW	10.3 μW	**160 nW**
Resolution(fF)	N/A	3.570	0.065	0.070	**6.0**
ENOB[1](bit)	6.83[3]	6.1	15.3	12.6	**13.3 ~ 14.2**
FoM[2](fJ/c-s)	7937	3936	7380	1360	**63.9[4]**

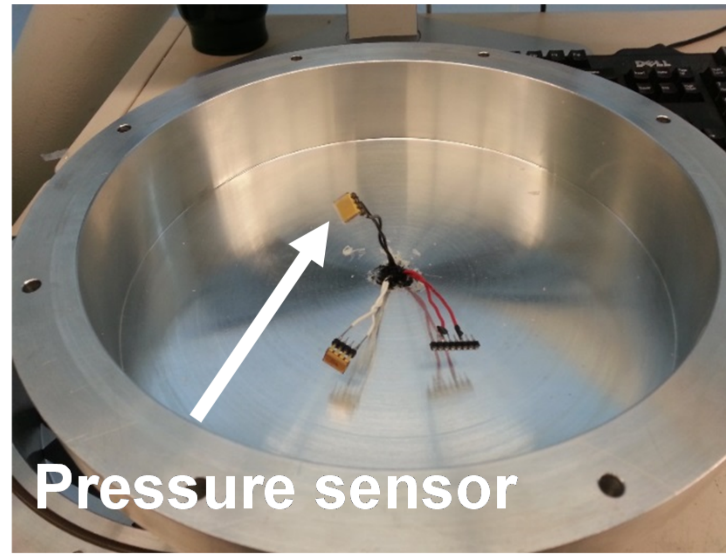
[1]ENOB = $(20 \times \log_{10}(Range/Resolution) - 1.76)/6.02$, [2]FoM = $(Power \times Tmeas)/2^{ENOB}$

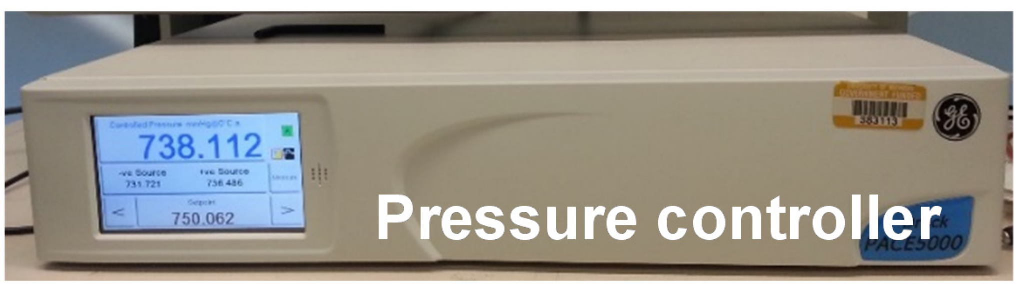
[3]This ENOB is obtained by applying sinusoidal signal to fixed capacitor.

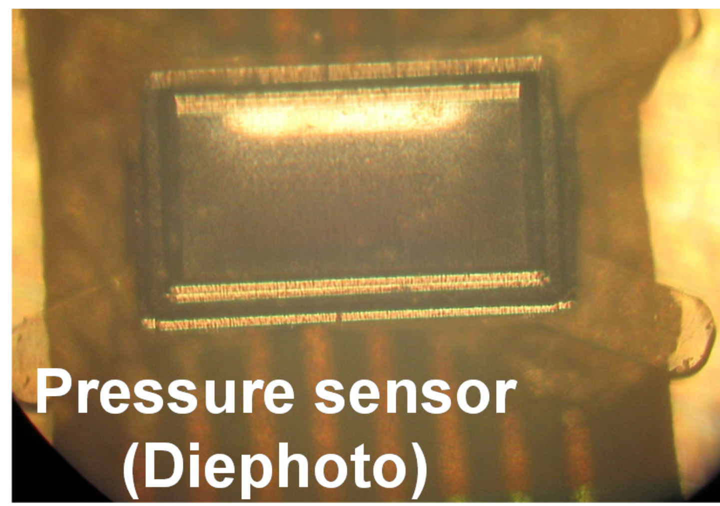
[4]This FoM is calculated by using lowest ENOB.

Testing Setup with Pressure Sensor

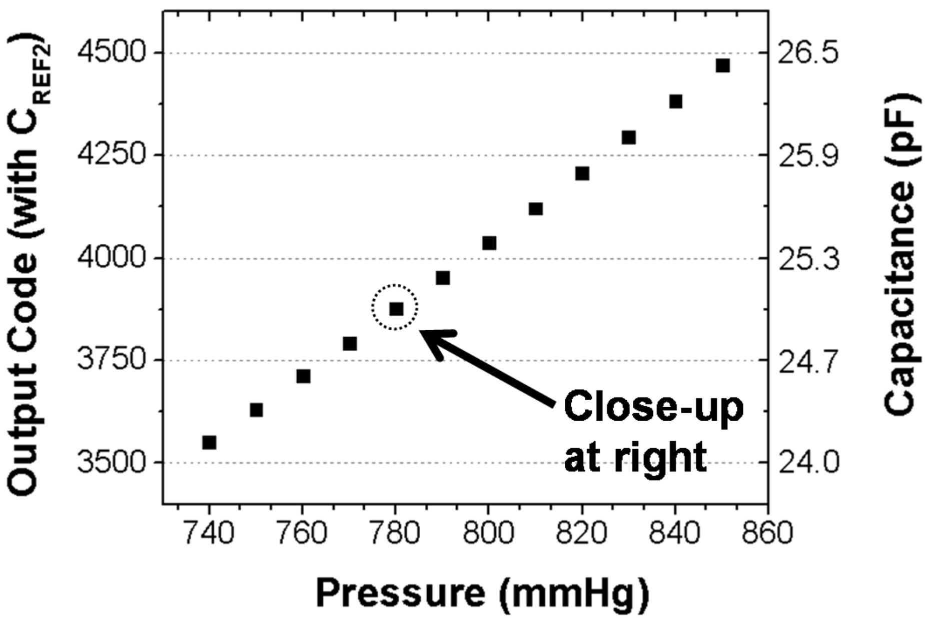


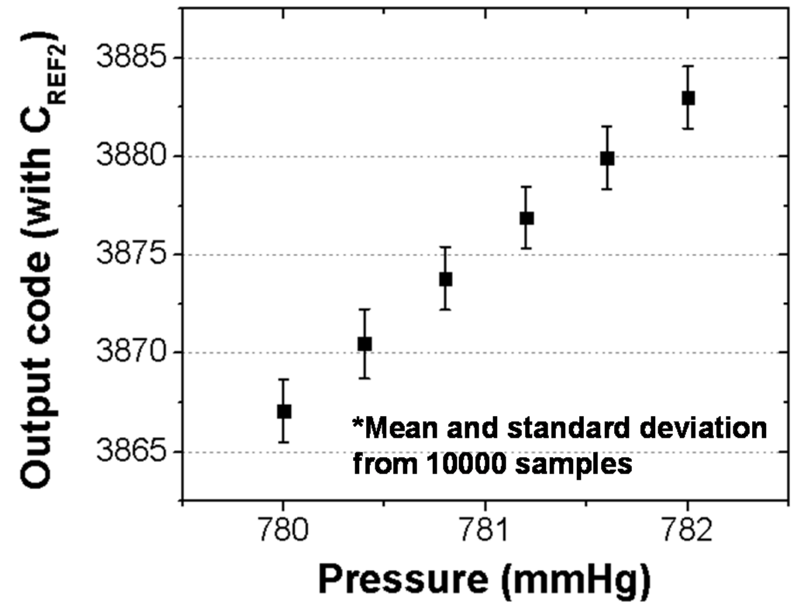






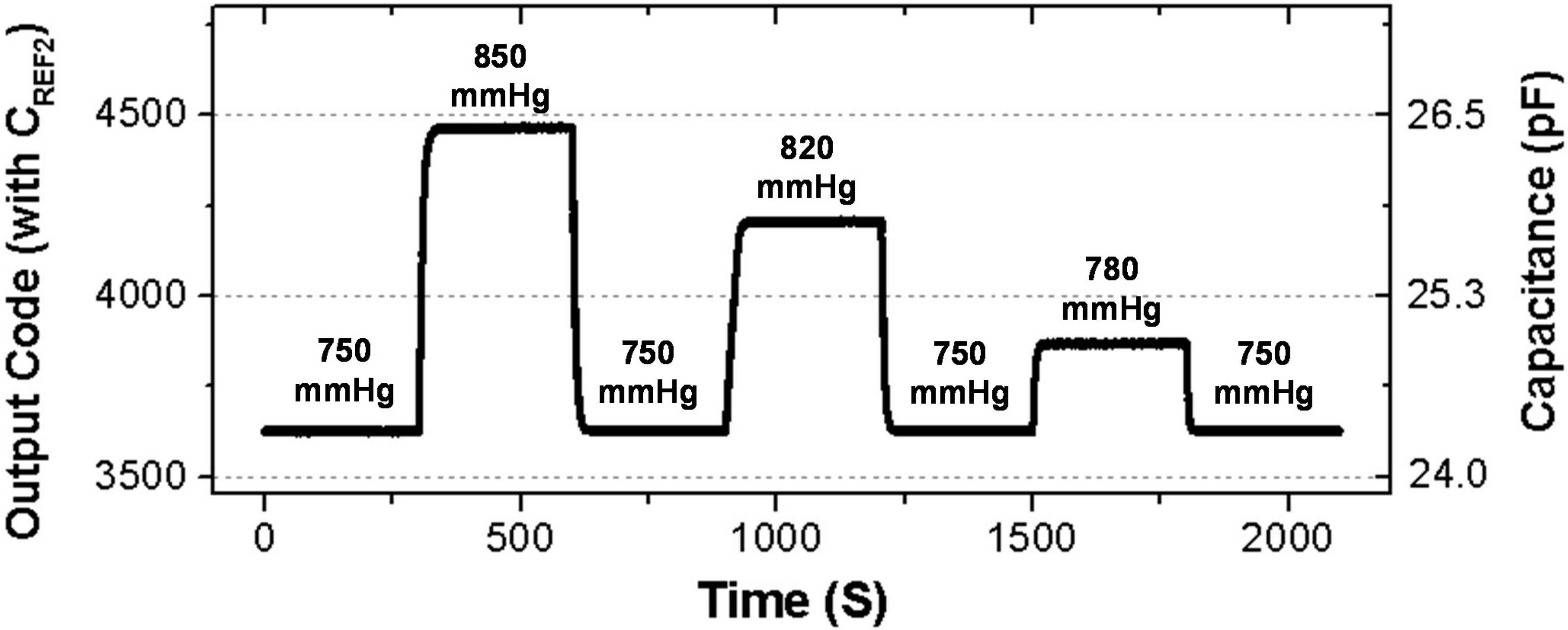
Testing with Pressure Sensor (Linearity)





- Linearity of $R^2 = 0.9997$
- Pressure resolution : 0.4mmHg(=2σ)

Testing with Pressure Sensor (Dynamic Behavior)



Conclusion

- **A CDC is proposed for ULP applications.**
  - Difference sampling CDS
  - CDS combined with SAR ADC for power saving
  - Conversion range extended using multiple references

- **Implementation Results**
  - Dissipates 160nW @ 250S/sec
  - 63.9fJ/conversion-step (20 x improved)
  - Verified with a pressure sensor

- **Promising for general-purpose sensor interface in ULP wireless sensor node**

A 0.85V 600nW All-CMOS Temperature Sensor with an Inaccuracy of ±0.4°C (3σ) from -40 to 125°C

Kamran Souri[1], Youngcheol Chae[2], Frank Thus[3], and Kofi Makinwa[1]

[1] Delft University of Technology, Delft, The Netherlands
[2] Yonsei University, Seoul, South Korea
[3] NXP Semiconductors, Eindhoven, The Netherlands

Sub-1V Temperature Sensing in CMOS?

With BJTs [Souri, JSSC '13]

✓ 1-point trim ⇒ ±0.2°C error (-55°C to 125°C)

✗ V_{BE} ~ 0.8V at -55°C

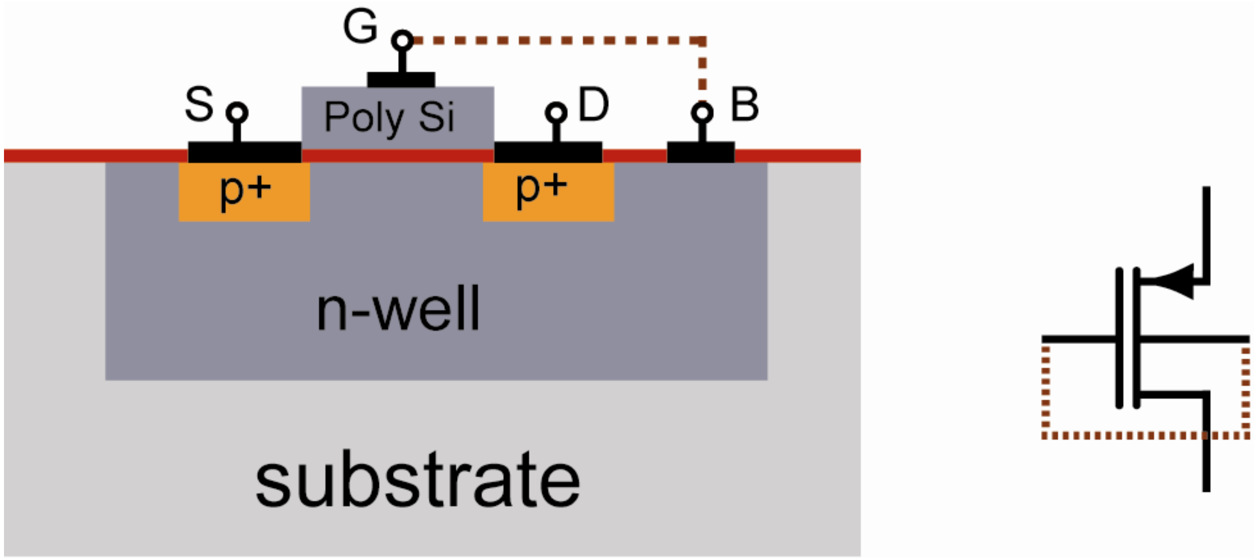
⇒ supply voltage > 1V

With MOSFETs [Chen, JSSC '10]

✓ V_{GS} ~ 0.4V at -55°C ⇒ sub-1V operation

✗ 2-point trim ⇒ ±0.5°C error (0°C to 90°C)

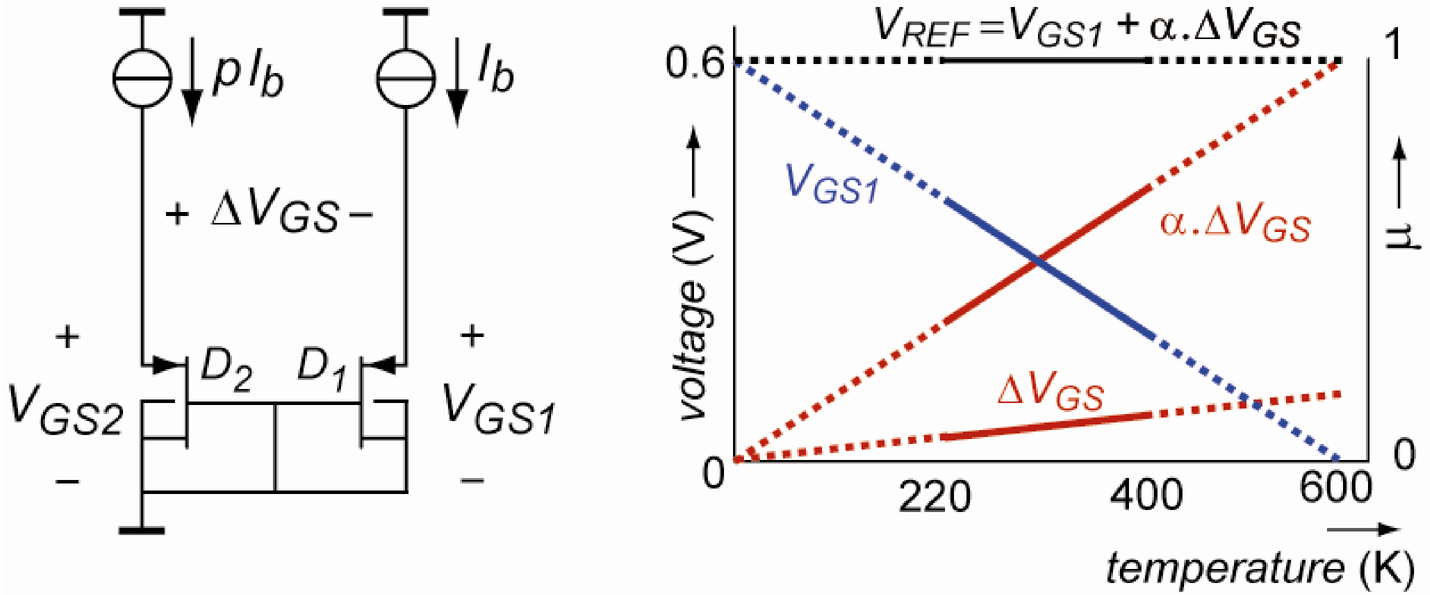
Dynamic Threshold MOST (DTMOST)



[Annema, JSSC '99]

- A standard P-type MOST
- BUT its body and gate terminals are tied together!
  $\Rightarrow$ near-ideal diode characteristic
  $\Rightarrow$ less spread [Souri, ESSCIRC '11] [Terauchi, JJAP '05]

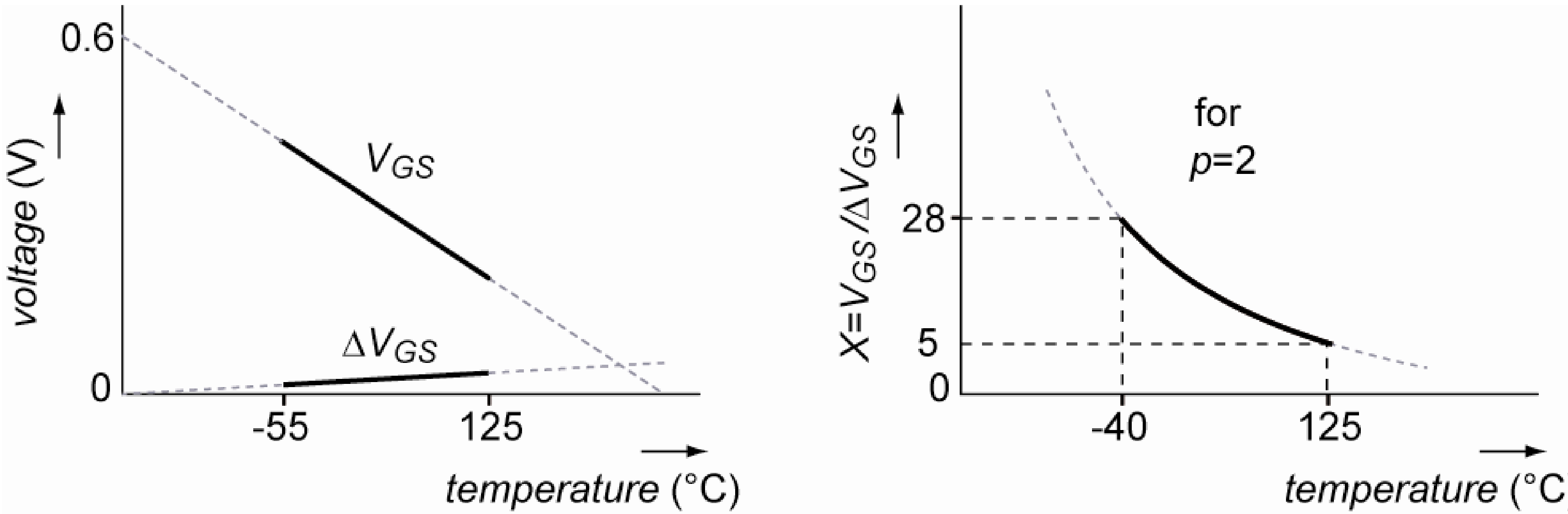
Operating Principle



- V_{REF} = temperature independent voltage (~0.6V)
  $\alpha \cdot \Delta V_{GS}$ = (linearly) temperature dependent voltage

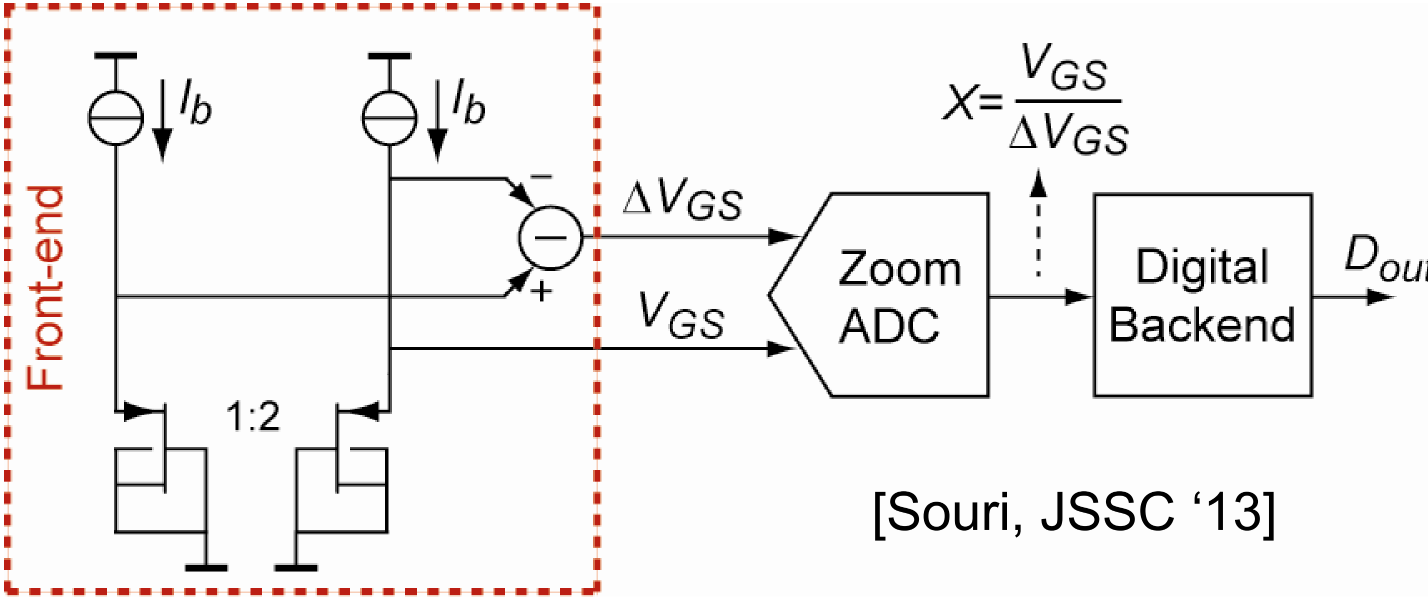
- Their ratio is a measure of temp: $\mu = \dfrac{\alpha.\Delta V_{GS}}{\underbrace{V_{GS} + \alpha.\Delta V_{GS}}_{\text{Reference}}}$

Efficient Sensing Principle



- V_{GS} and ΔV_{GS} are both temperature dependent
- So $X=V_{GS}/\Delta V_{GS}$ is a monotonic function of temperature
- Which is easily linearized: $\mu = \dfrac{\alpha}{X+\alpha} = \dfrac{\alpha \cdot \Delta V_{GS}}{\underbrace{V_{GS}+\alpha \cdot \Delta V_{GS}}_{\text{BG Reference}}}$

Simplified Block Diagram



- Linearization in Digital Backend: $\mu = \frac{\alpha}{X + \alpha}$
- Digital $\alpha \Rightarrow$ accurate (trim knob)

Front-End

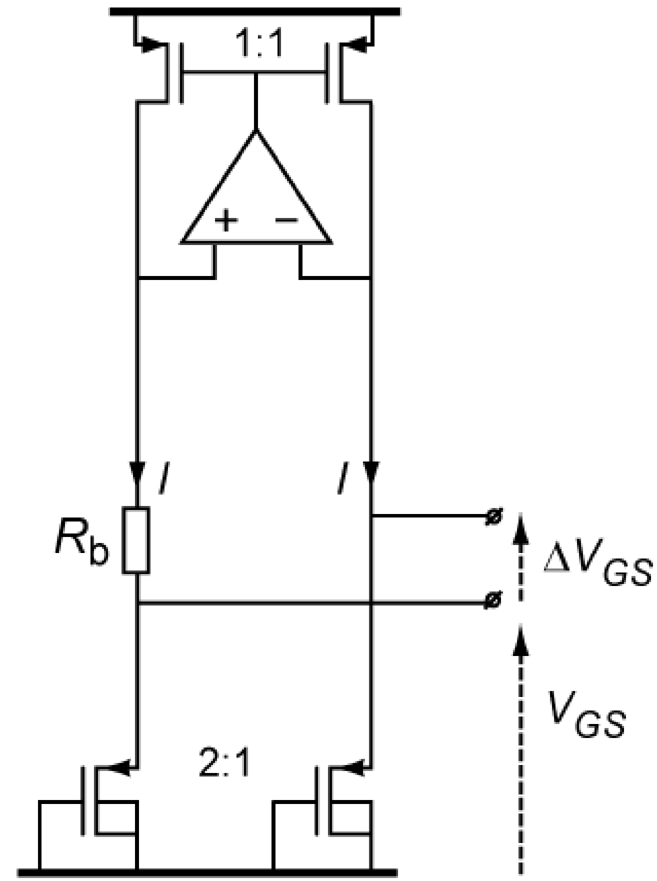
- Opamp forces ΔV_{GS} across R_b

  $\Rightarrow$ I is a PTAT current

- Power & energy efficiency

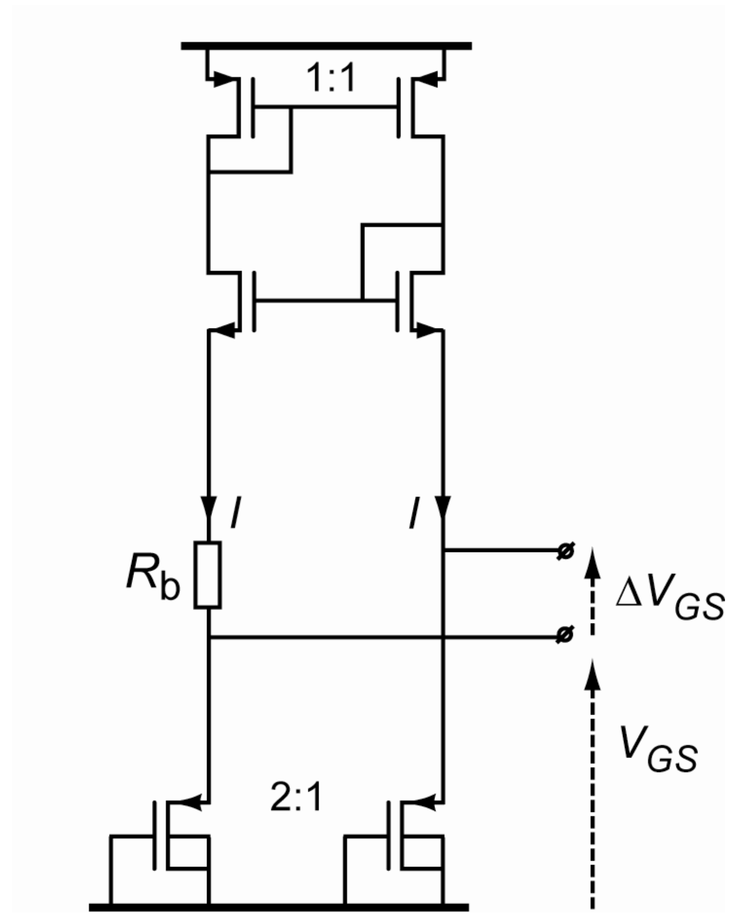
  $\Rightarrow$ 2:1 area ratio

- Opamp's supply current?



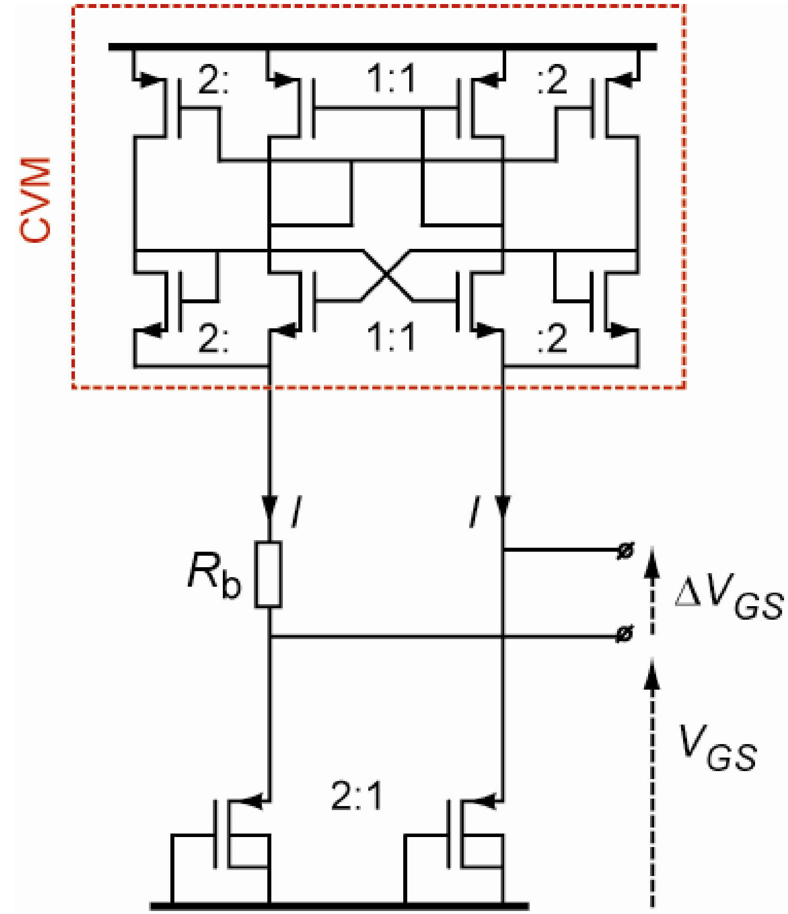
Power Efficient Front-End (1)

- Current-voltage mirror re-uses DTMOST's bias current
- $2V_{GS,SUB} + V_{DS,SAT} < 1V$
- BUT low loop gain
  $\Rightarrow$ low CMRR?



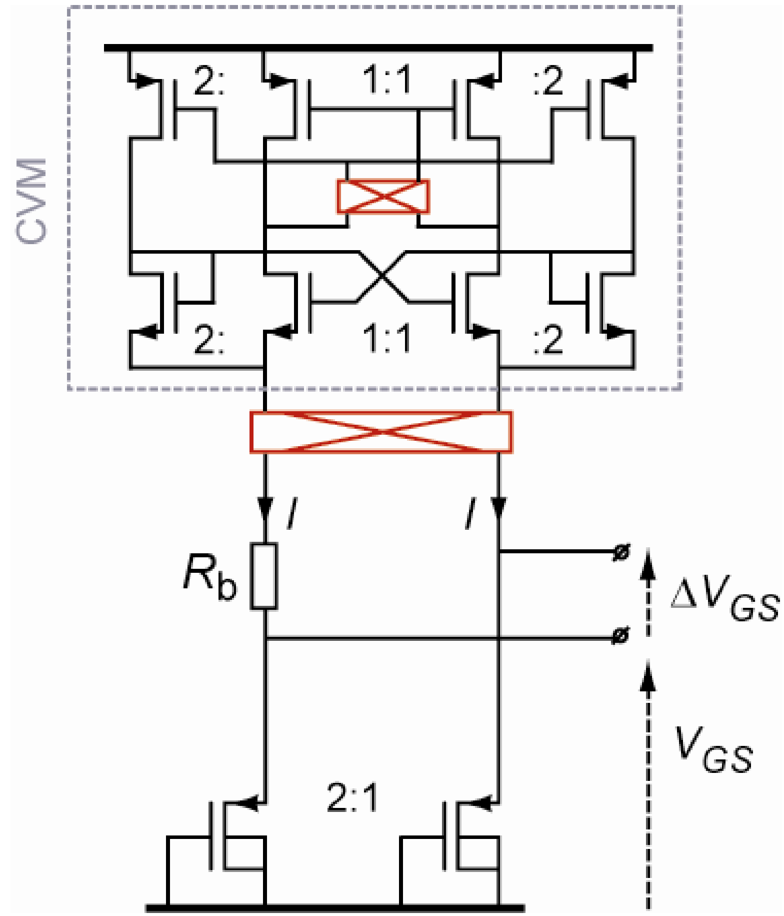
Power Efficient Front-End (2)

- Improved current-voltage mirror [Lam, VLSI'10]
- Same headroom
- Positive feedback loop enhances loop gain



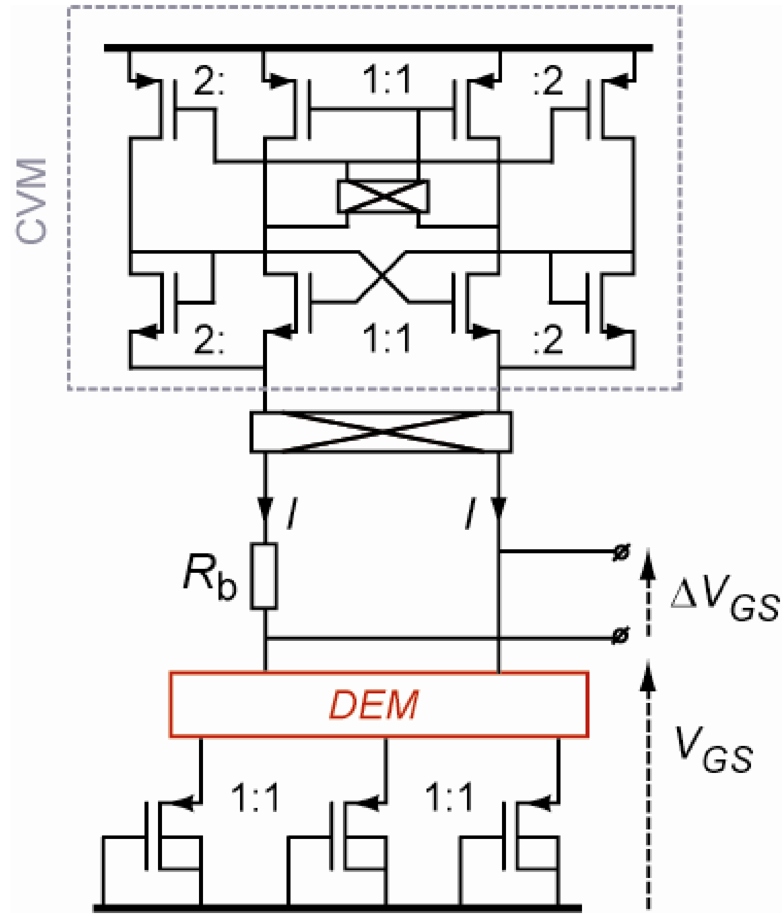
Offset Cancellation

- Input-referred offset modifies the bias current and thus V_{GS}
- Chopping removes the offset

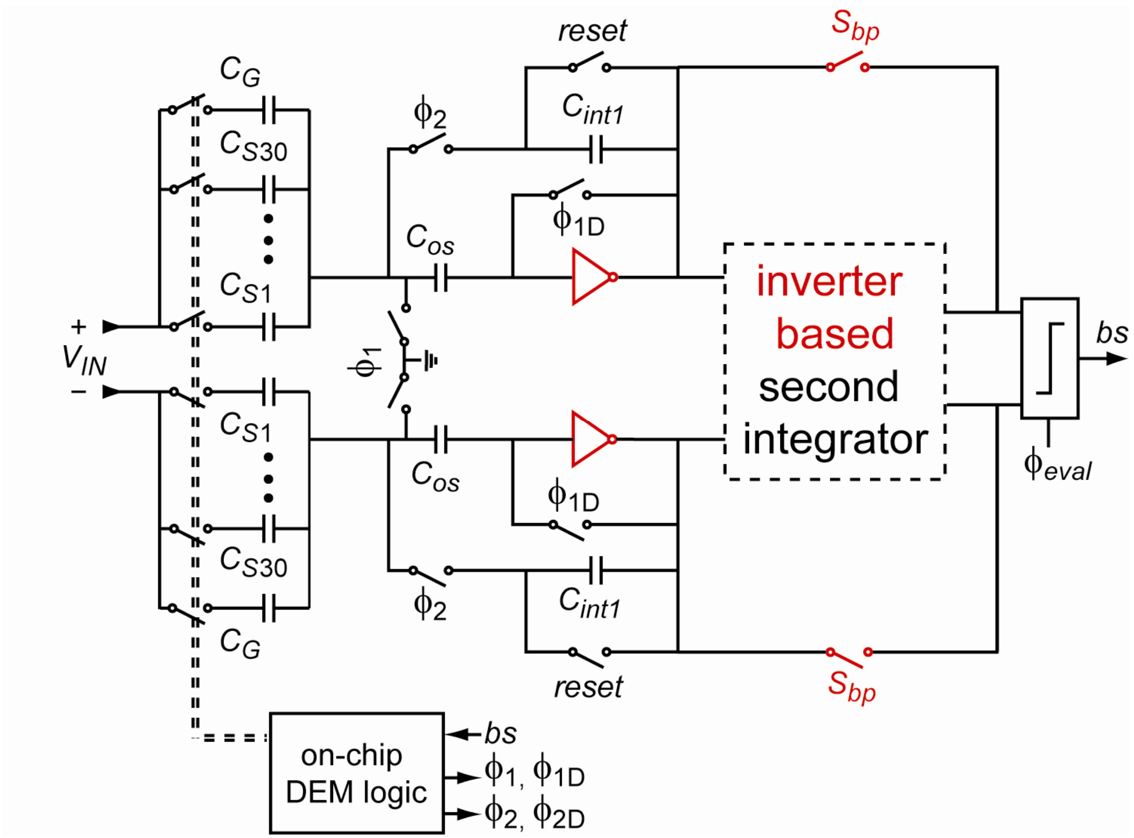


DEM Establishes Accurate ΔV_{GS}

- 3 identical DTMOSTs establish a 1:2 area ratio
- DEM with Kelvin-connected switches $\Rightarrow$ Accurate ΔV_{GS}



Inverter-Based Zoom ADC

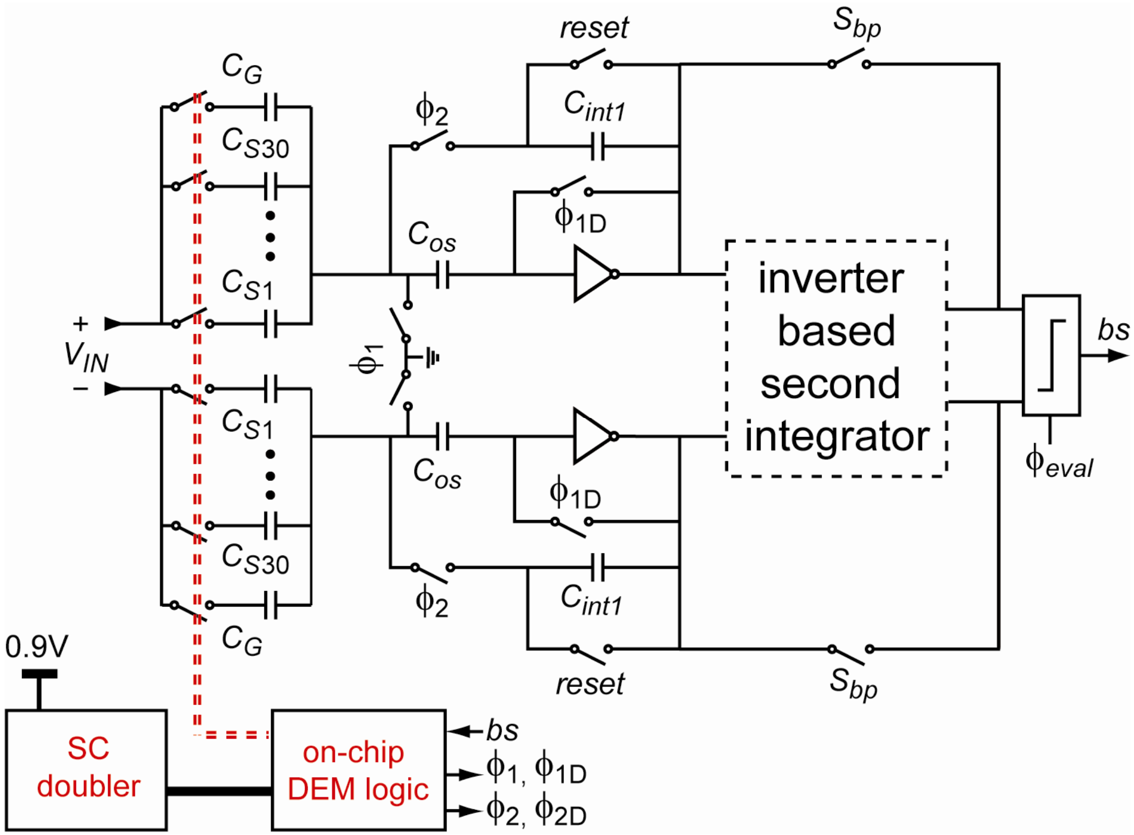


1st stage: 135nA

2nd stage: 65nA

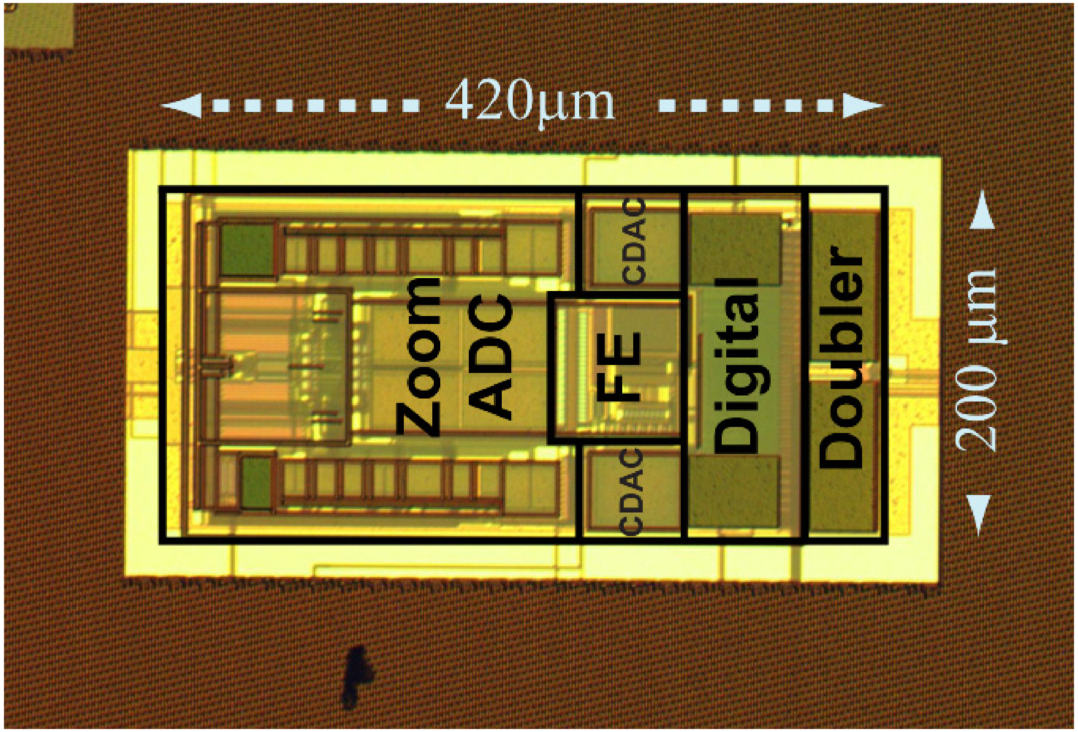
- SAR-assisted 2nd-order ΣΔ ADC [Souri, JSSC'13]
- Inverter-based OTAs ⇒ sub-1V, low-power operation

Inverter-Based Zoom ADC



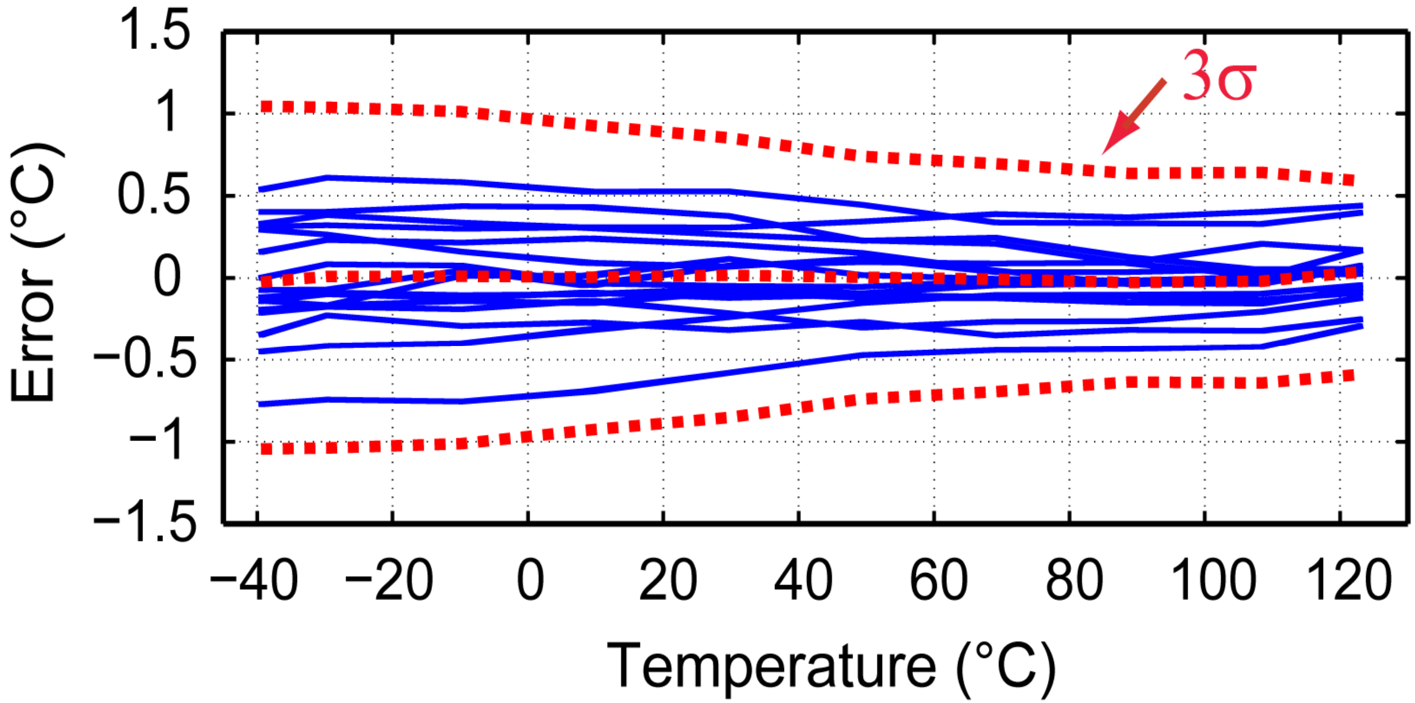
- SC doubler ⇒ ~1.8V supply to drive V_{GS} switches

Chip Micrograph



- 0.16μm CMOS
- 0.085mm^2 (active area)
- Supply voltage:
  Analog: 0.85-1.2V
  Digital: 1V
- Supply current:
  700nA (with digital)

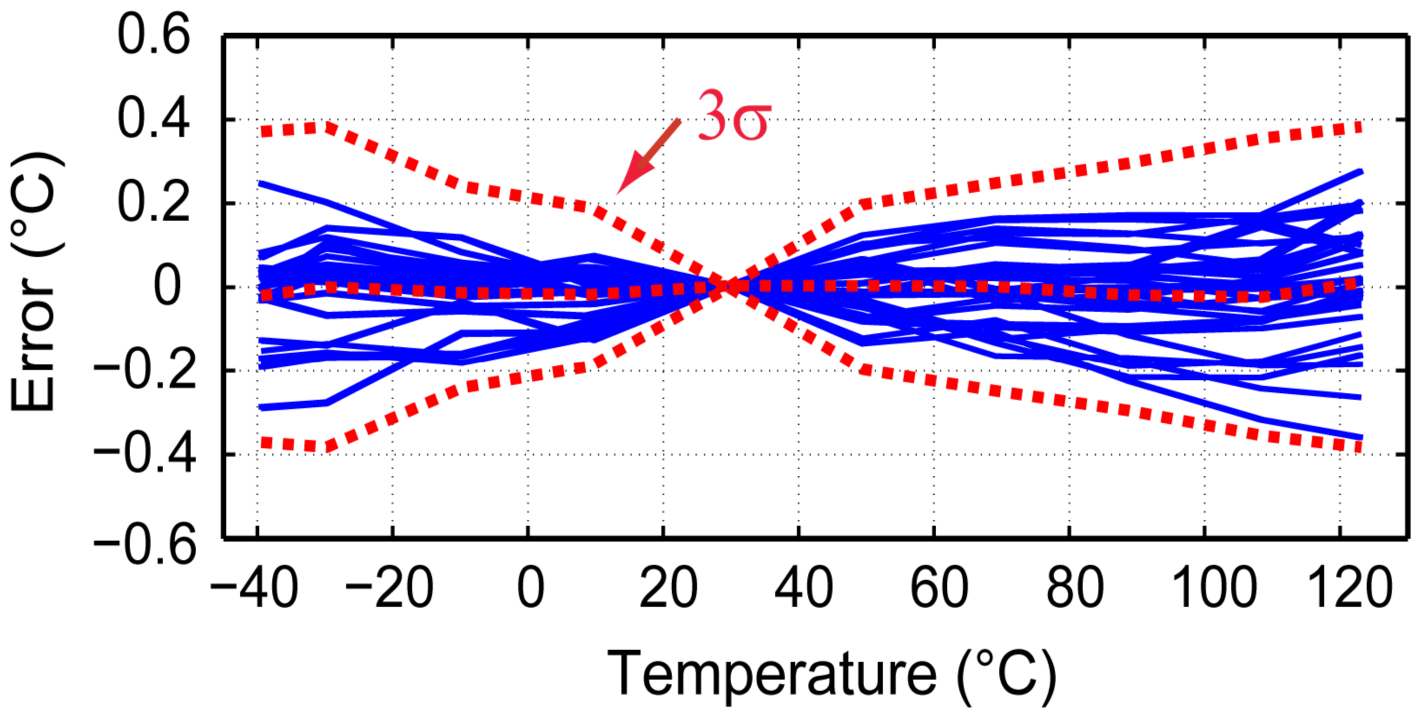
Untrimmed Spread



16 devices, one batch

- After batch-calibration: ±1°C (3σ)

Alpha-Trimmed Spread



16 devices, one batch

- After correcting for systematic non-linearity (< ±0.1°C)
- Single alpha trim at 30°C ⇒ ±0.4°C (3σ)

Comparison to Prior Art

	This work	Souri JSSC-13	Law JSSC-10
Sensor type	**DTMOST**	BJT	MOST
Supply current	**700nA**	3.4μA	190nA
Supply voltage	**0.85-1.2V**	1.5-2V	0.5V (sensor) 1V (digital)
Temp. range	**-40 – 125°C**	-55 – 125°C	-10 – 30°C
Inaccuracy (Trim)	**±0.4°C (3σ) 1-point**	±0.15°C (3σ) 1-point	-0.8°C / 1°C 2-point
Relative inaccuracy	**0.48%**	0.2%	4.5%
Resolution (T_{conv})	**0.063°C (6msec)**	0.02°C (5.3msec)	0.2°C (30msec)

Sub-1V, sub-μW operation and 10x more accuracy!

Conclusions

- DTMOSTs ⇒ accuracy and sub-1V operation

- Inverter-based OTAs ⇒ sub-1V, low-power readout
- Voltage doubler ⇒ sub-1V sampling-switch drive

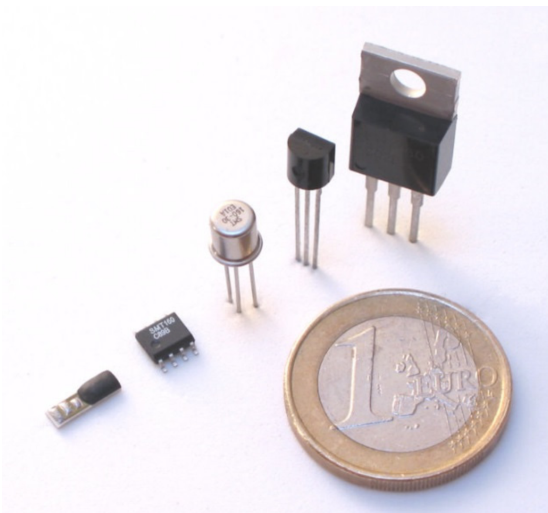
- Result is a sub-1V, sub-μW, all-CMOS temp sensor with state-of-the-art accuracy: ±0.4°C using a 1-point trim

A BJT-based CMOS Temperature Sensor with a 3.6pJ°C^2 Resolution FoM

A. Heidary, G. Wang
K.A.A. Makinwa and G.C.M. Meijer

Smartec, The Netherlands
Delft University of Technology, The Netherlands

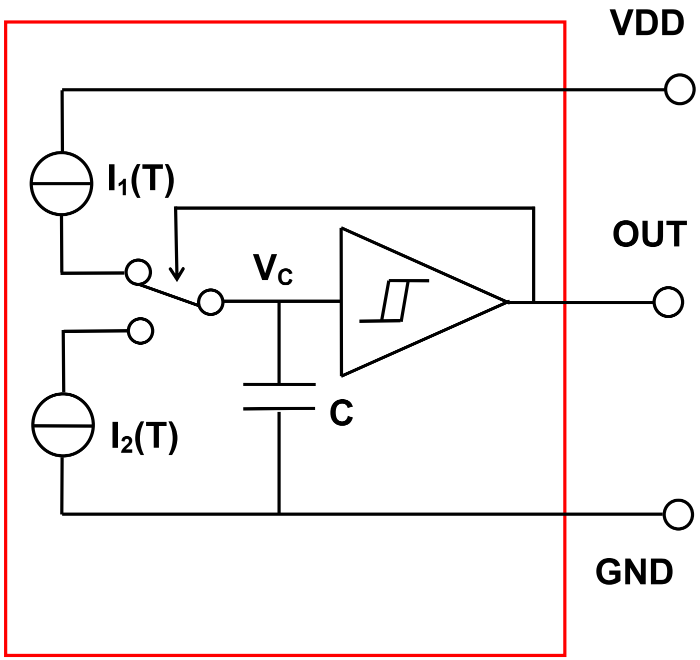
Design target ------- modernize the successful SMT-160

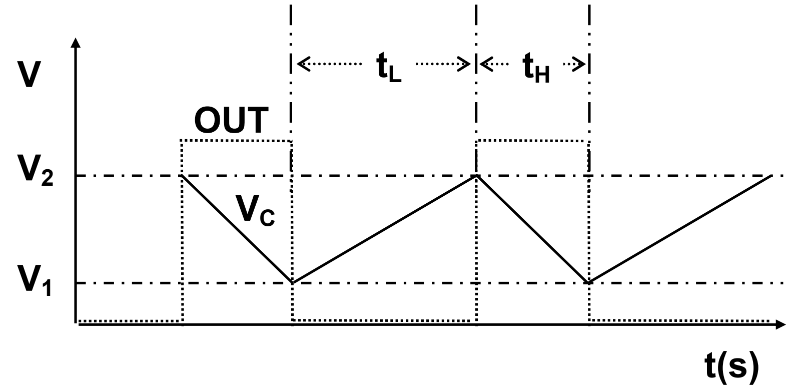


Temperature range	-45ºC to 130ºC
accuracy (trim method)	±1.2ºC (1-point)
Resolution measurement time	0.005ºC 20ms
Technology chip area	2.4µm BiCMOS 5mm^2

Challenge: Achieve the same or better performances in low cost CMOS

Basic operation of temperature sensor





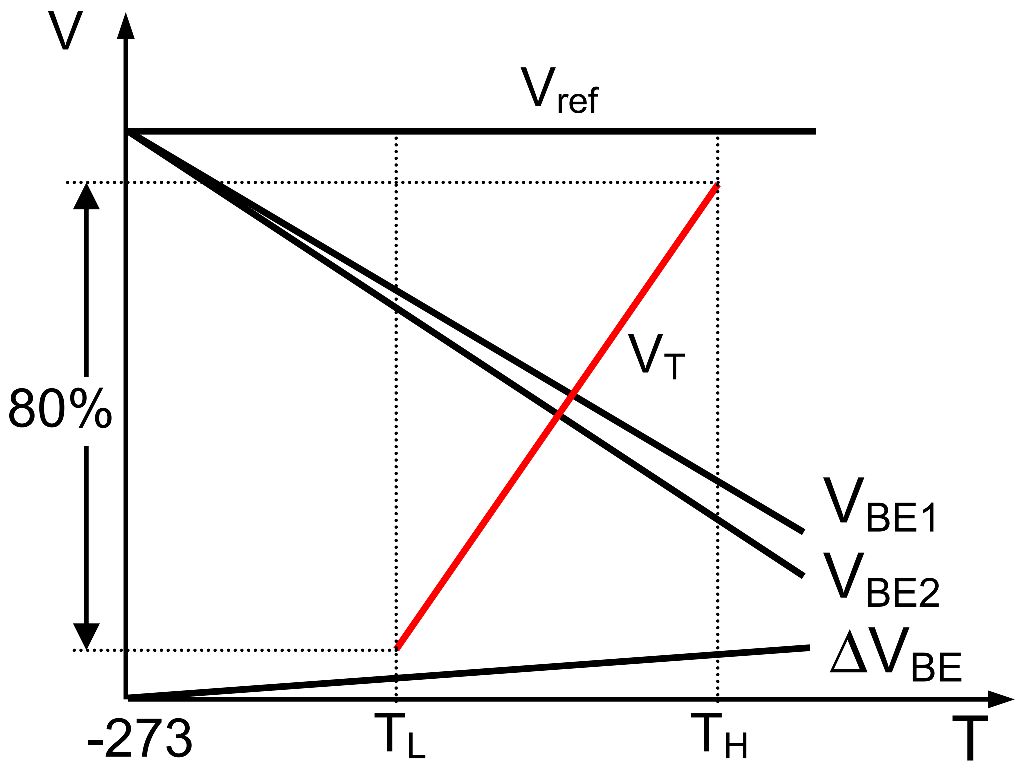
$$t_L = \frac{(V_2 - V_1) \times C}{I_1(T)} \qquad t_H = \frac{(V_2 - V_1) \times C}{I_2(T)}$$

$$\left.\begin{array}{r} I_1 \propto T \\ I_1 + I_2 = \text{constant} \end{array}\right\} \Rightarrow \boxed{D = \frac{t_H}{t_L + t_H} = \frac{I_1}{I_1 + I_2} \propto T}$$

☺ D is insensitive to V_1, V_2 and C

V_{BE} and ΔV_{BE} from BJTs

- V_{BE}: CTAT (Complementary To Absolute Temperature)
- ΔV_{BE}: PTAT (Proportional To Absolute Temperature)



$$V_{ref} = V_{BE} + K_1 \Delta V_{BE}$$

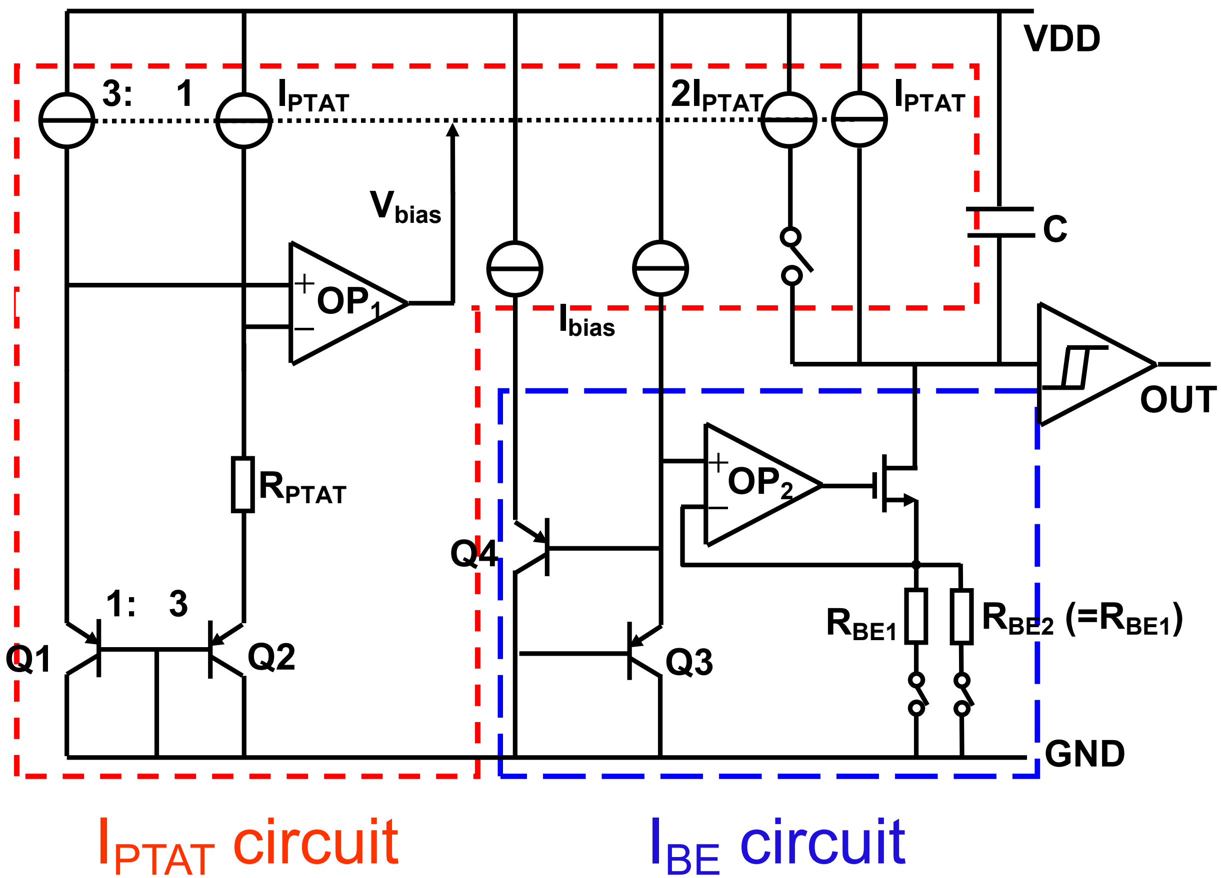
Band-gap reference

$$V_T = K_2 \Delta V_{BE} - K_3 V_{BE}$$

Positive *T* coefficient

$$V_T / V_{ref} \propto T$$

Simplified schematic diagram of the CMOS SMT



$V_{BE1}, V_{BE2} \Rightarrow I_{PTAT}$

$V_{BE3} \Rightarrow I_{BE}$

$I_1 = 3I_{PTAT} - 0.5I_{BE}$

$I_2 = I_{BE} - I_{PTAT}$

$I_1 \propto V_T$

$I_1 + I_2 \propto V_{ref}$

$$D = \frac{I_1}{I_1 + I_2} = \frac{3I_{PTAT} - 0.5I_{BE}}{0.5I_{BE} + 2I_{PTAT}}$$

Error source 1: component mismatch

☹ Offset in OP_1 and OP_2 ➡ ☺ <u>Chopping</u> for op-amps

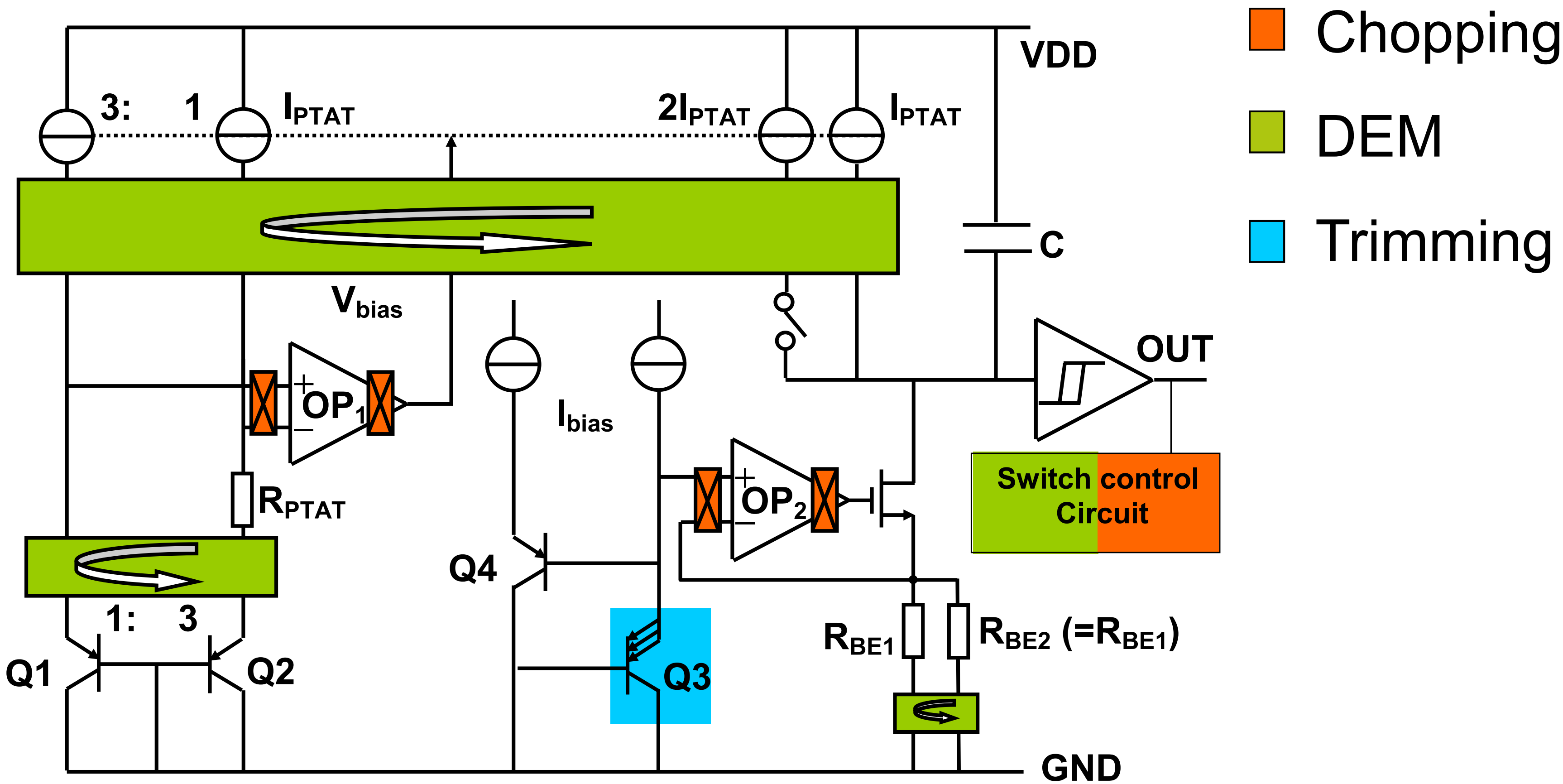
☹ Ratio errors in current mirror, BJTs and resistors ➡ ☺ <u>Dynamic Element Matching</u> (DEM)

Chopping & DEM ➡ Averaging ➡ Error = Second order residual

Error source 2: PTAT spread of V_{be3}

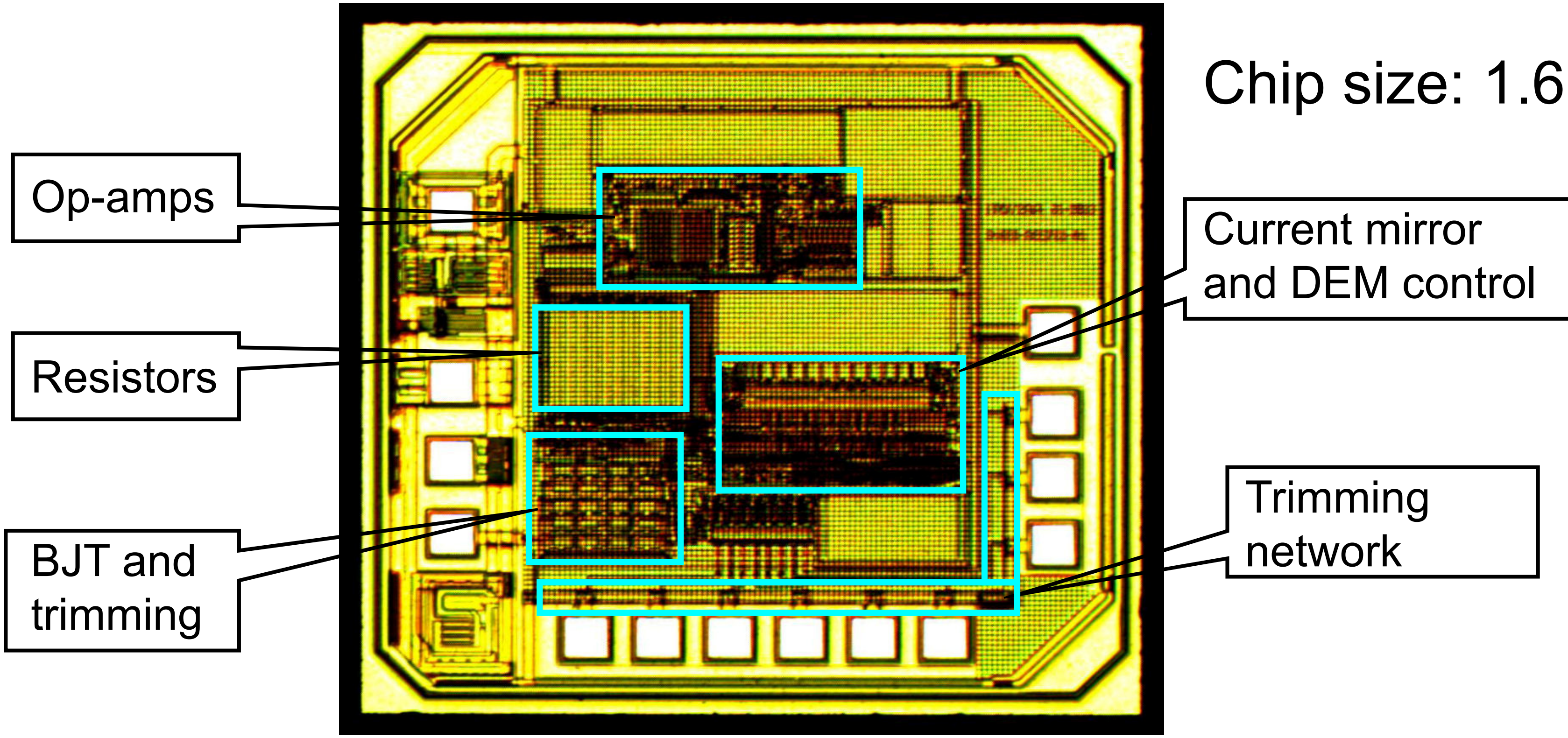
☺ <u>One-point trim</u> can adjust $V_{be3}(T_r)$ to its nominal value

Design for accuracy



- Chopping and DEM state machines are self clocked
- A complete DEM cycle includes 8 periods

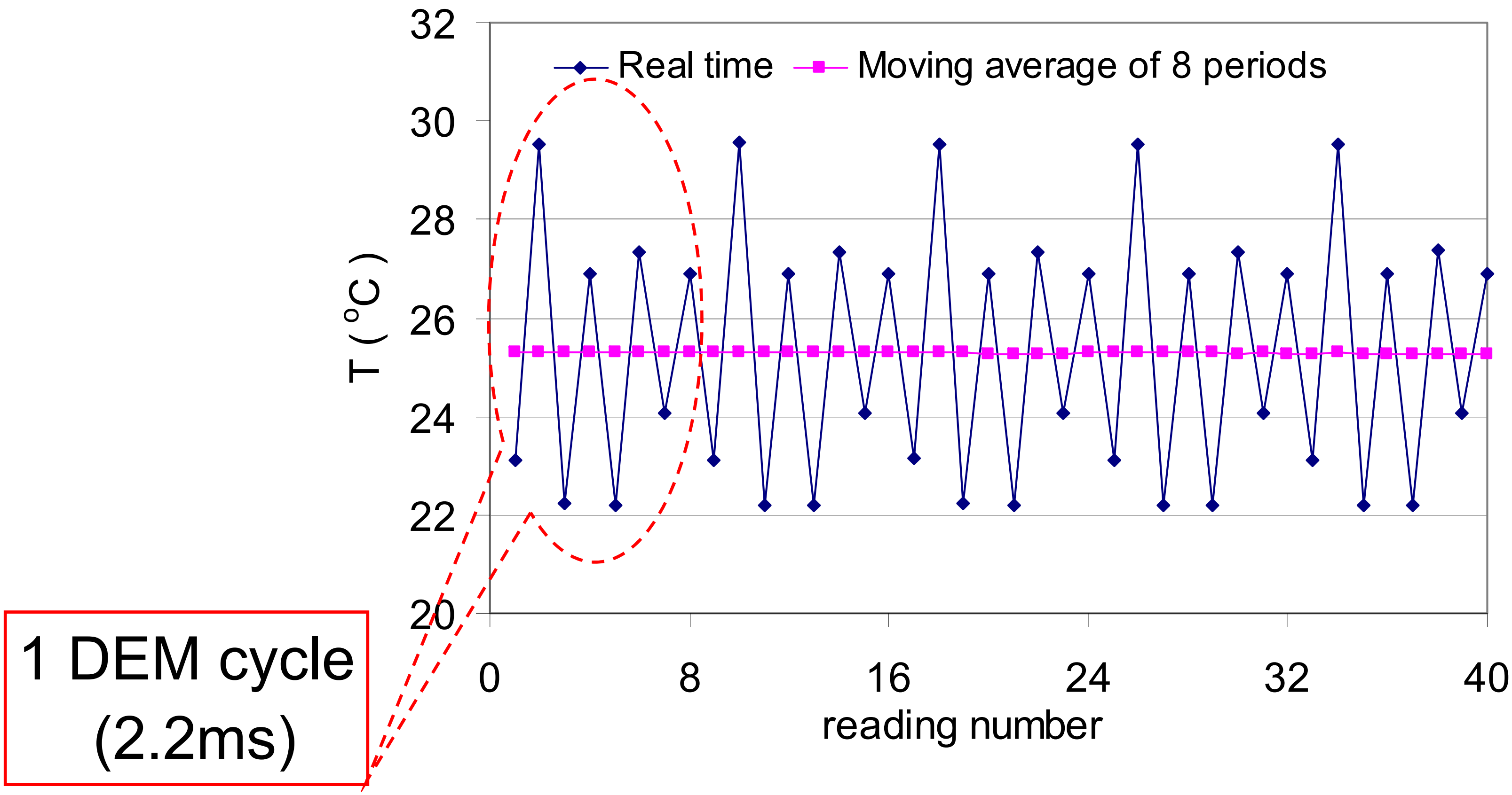
Implementation in 0.7μm CMOS



Chip size: 1.6mm^2

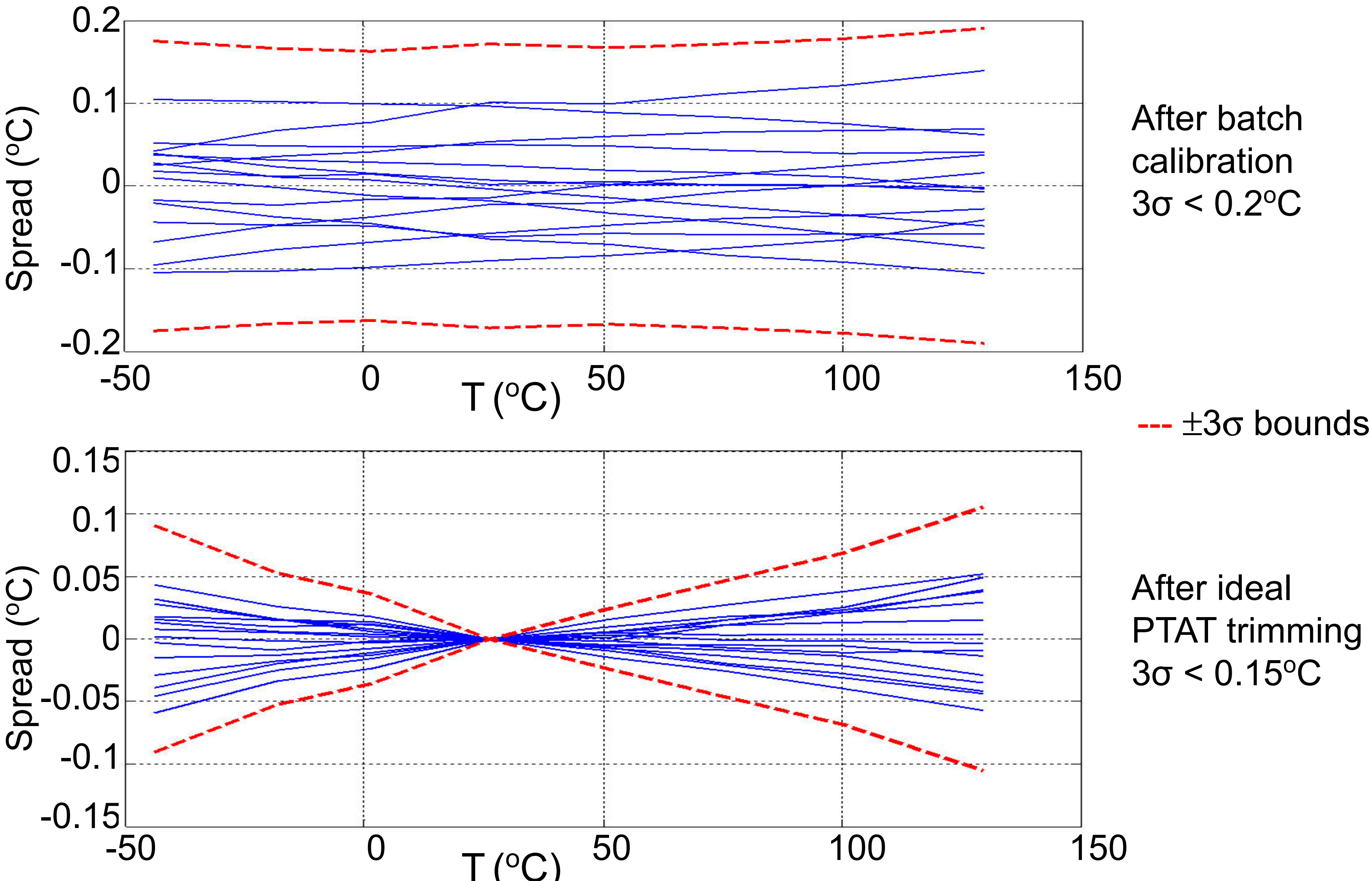
Supply voltage	2.9V to 5.5V
Supply current (25°C)	53μA to 68μA
Single period (25°C)	235μs to 670μs
Packaged pins	VDD GND OUT

Real time output and after average

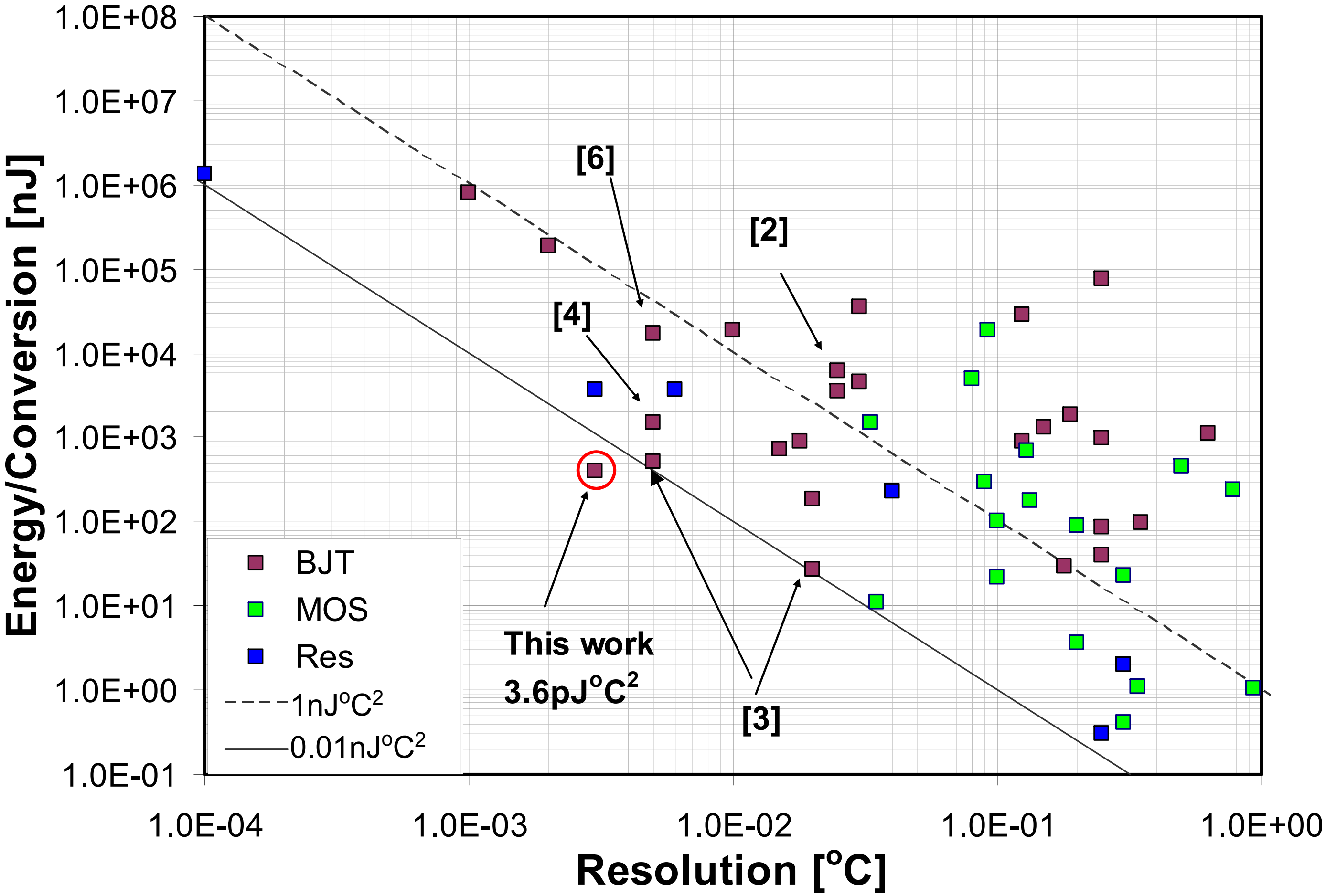


- Duty cycle of 1 period: σ = 2.74 K
- Moving average over 8 periods: σ = 0.003 K

Spread of 15 samples



Energy/Conversion vs. Resolution*



- Resolution FoM = (Energy/Conversion) × Resolution^2
- This work is 3x improvement on state of the art

* K.A.A. Makinwa, "Smart Temperature Sensor Survey", [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls

Comparison to prior art

	This work	SMT-160 [6]	Heidary [4]	Souri [3]	Aita [2]
Technology	0.7µm CMOS	2.4µm BiCMOS	0.13µm CMOS	0.16µm CMOS	0.7µm CMOS
Temperature range (ºC)	-45 to 130	-45 to 130	-55 to 85	-55 to 125	-55 to 125
Spread (ºC) (trim method)	±0.15 [1] (1-point)	±1.2 [2] (1-point)	±0.15 [1] (1-point)	±0.15 [1] (1-point)	±0.1 [1] (1-point)
Resolution (ºC) measurement time (ms)	0.003 [3] 2.2	0.005 20	0.005 20	0.02 5.3	0.025 100
Resolution FoM (pJºC^2)	3.6	430	41	11	3900

[1] 3σ [2] Maximum [3] V_{dd}=3.3V

Conclusion: our design target has been achieved

Conclusions

A BJT-based temperature sensor with a Duty-Cycle modulated output has been implemented in 0.7μm CMOS

➢ Errors are reduced by
  - Chopping and DEM
  - One point trimming

☺ Spread less than 0.15ºC

☺ Resolution 0.003ºC in 2.2ms

☺ Res. FoM = 3.6pJºC^2, 3x improvement on state of the art

☺ The design is ready for production

A 1.55x0.85mm² 3ppm 1.0μA 32.768kHz MEMS-based Oscillator

Samira Zali Asl[1,2],
Shouvik Mukherjee[1], Will Chen[1], Kimo Joo[1],
Rajkumar Palwai[1], Niveditha Arumugam[1], Preston Galle[1],
Meghan Phadke[1], Charles Grosjean[1], Jim Salvia[1], Hae-chang Lee[1],
Sudhakar Pamarti[3], Terri Fiez[2], Kofi Makinwa[4], Aaron Partridge[1], Vinod Menon[1]

[1] SiTime Corporation, Sunnyvale, CA
[2] Oregon State University, Corvallis, OR
[3] University of California, Los Angeles, CA
[4] Delft University of Technology, Delft, The Netherlands

SiTime™

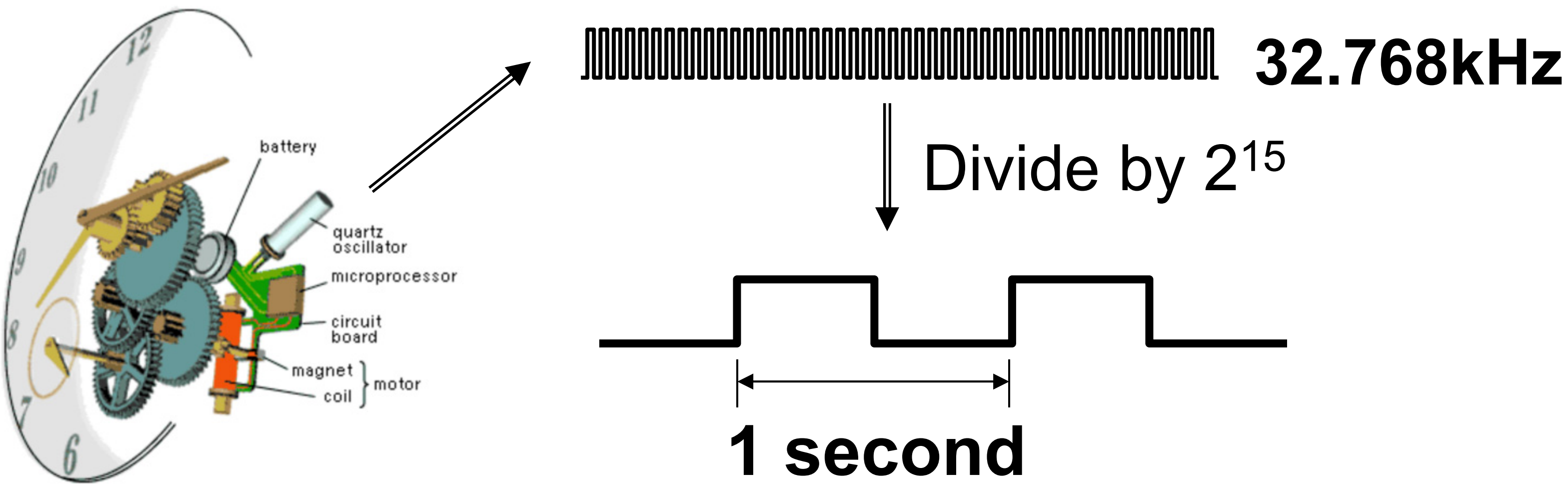
Revolution in Computing Devices

Vatican City: 2005 vs. 2013

Wearable devices coming next
Small size and low power

Timing Reference

- 32.768kHz clock for time keeping

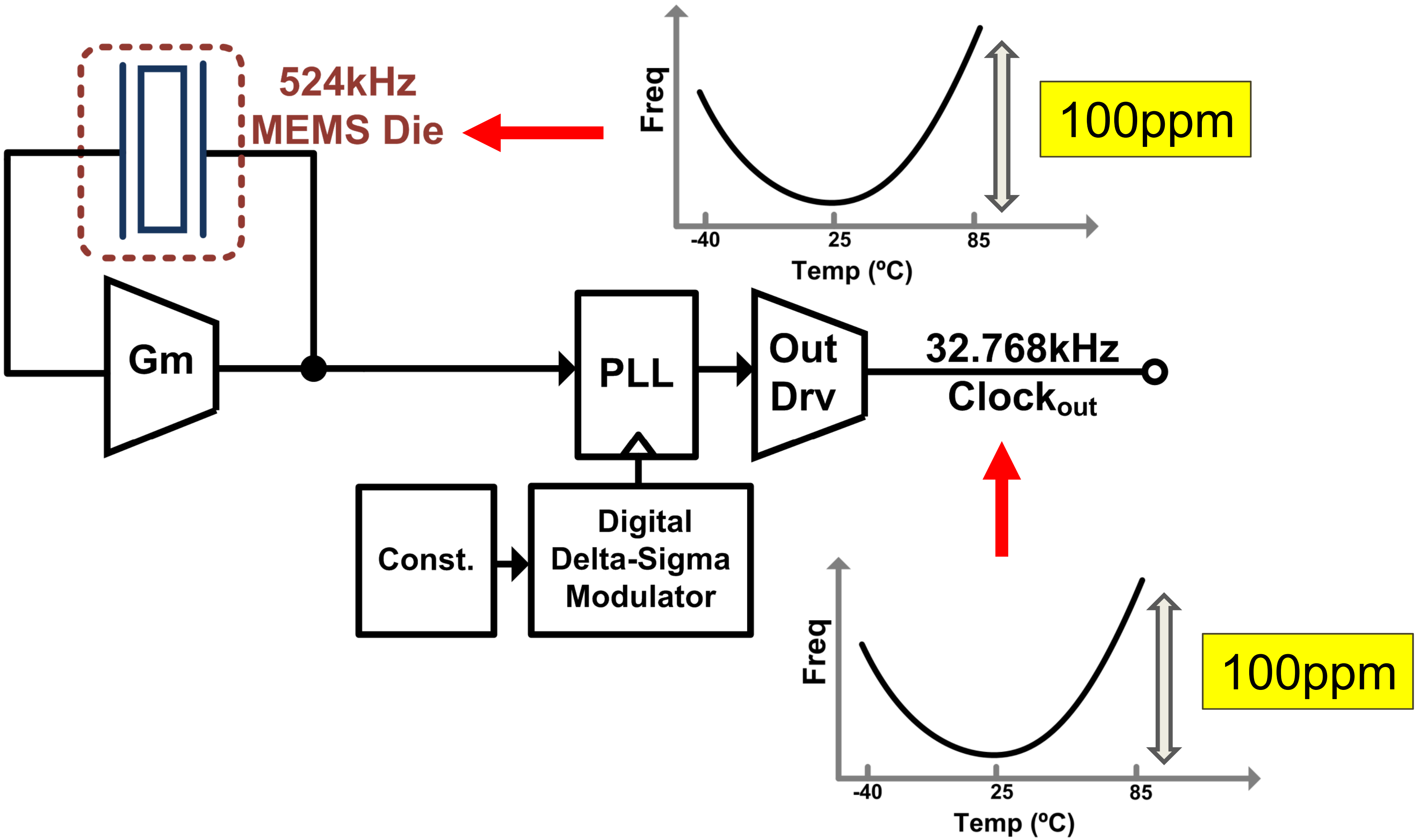


Requirements		Solution
Small Size	→	MEMS Technology
Low power	→	+ CMOS Techniques
High Accuracy	→	+ Temp. Comp. Engine

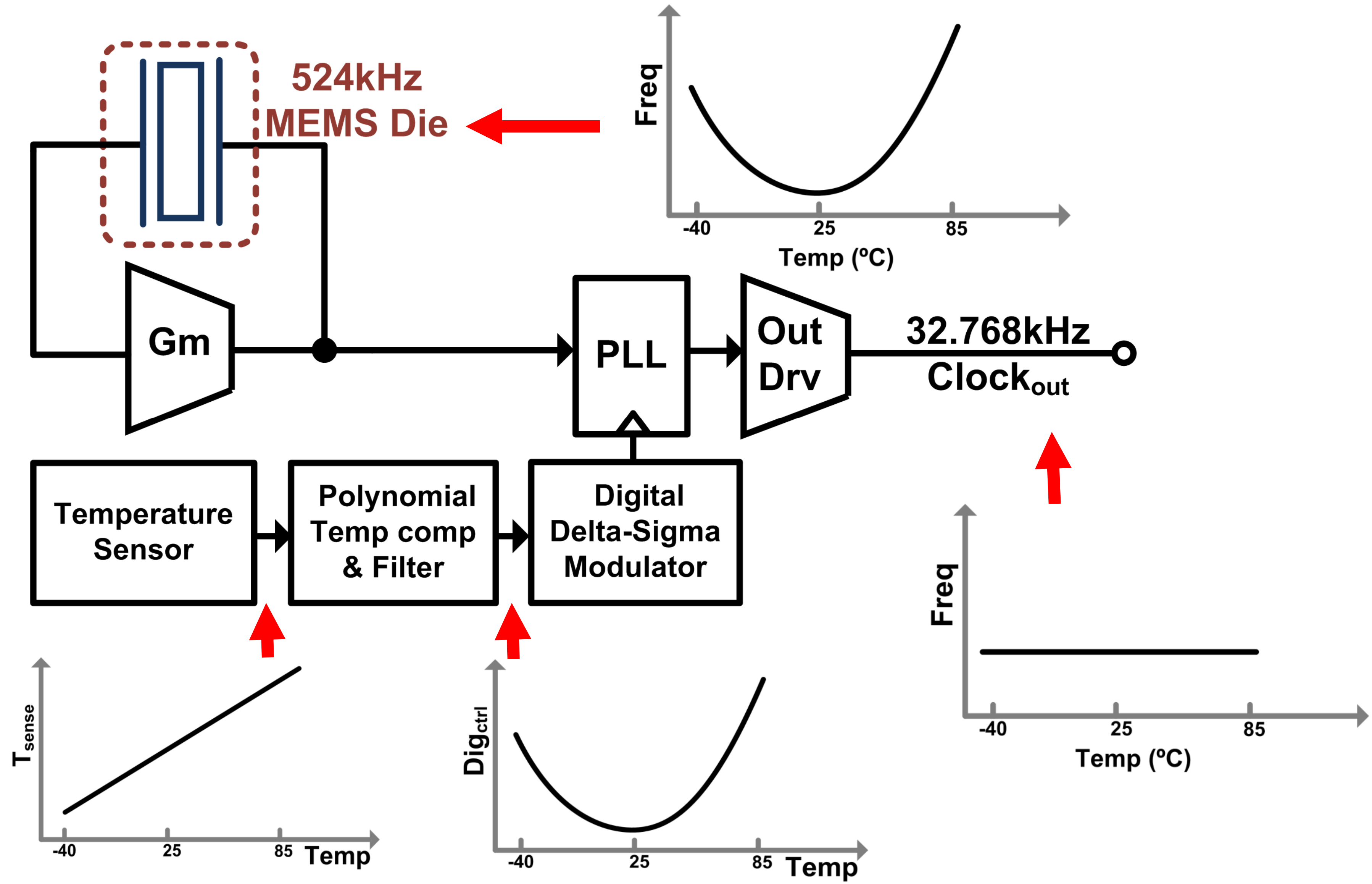
Outline

- Motivation
- **System Level Overview**
- Block Level Design
- Measurement Results
- Conclusion

MEMS-based 32kHz Oscillator (XO)



MEMS-based 32kHz Oscillator (TCXO)

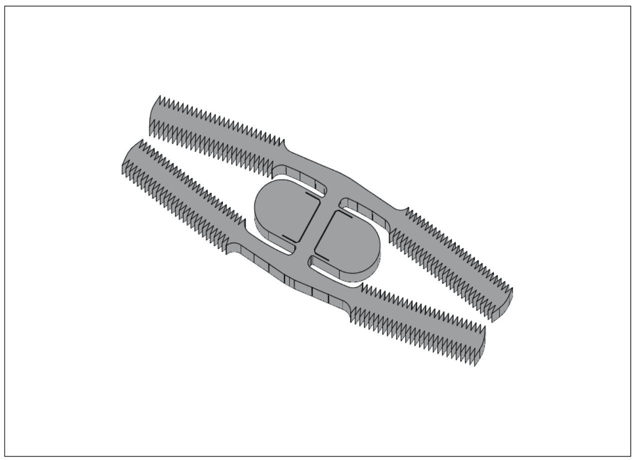


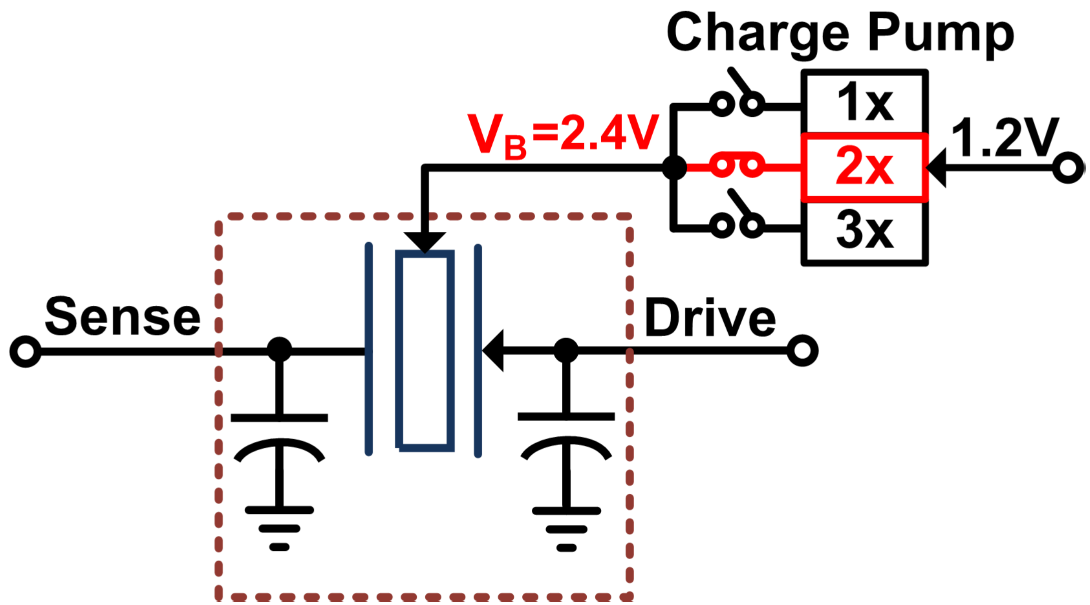
Outline

- Motivation
- System Level Overview
- **Block Level Design**
  - **MEMS Resonator & its Sustaining Oscillator**
  - Phase Locked Loop (PLL)
  - Temperature to Digital Converter (TDC)
  - Voltage Regulators
  - Output Driver
- Measurement Results
- Conclusions

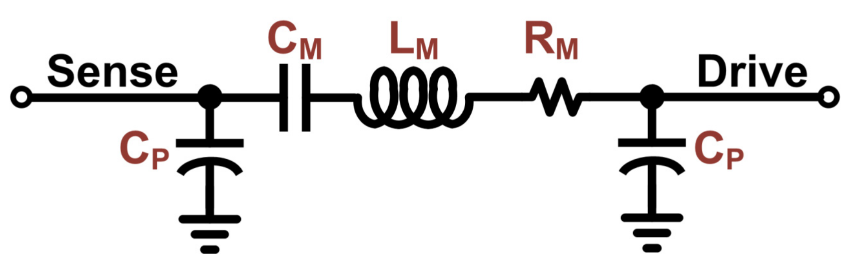
MEMS Resonator

Tuning-fork
524kHz MEMS





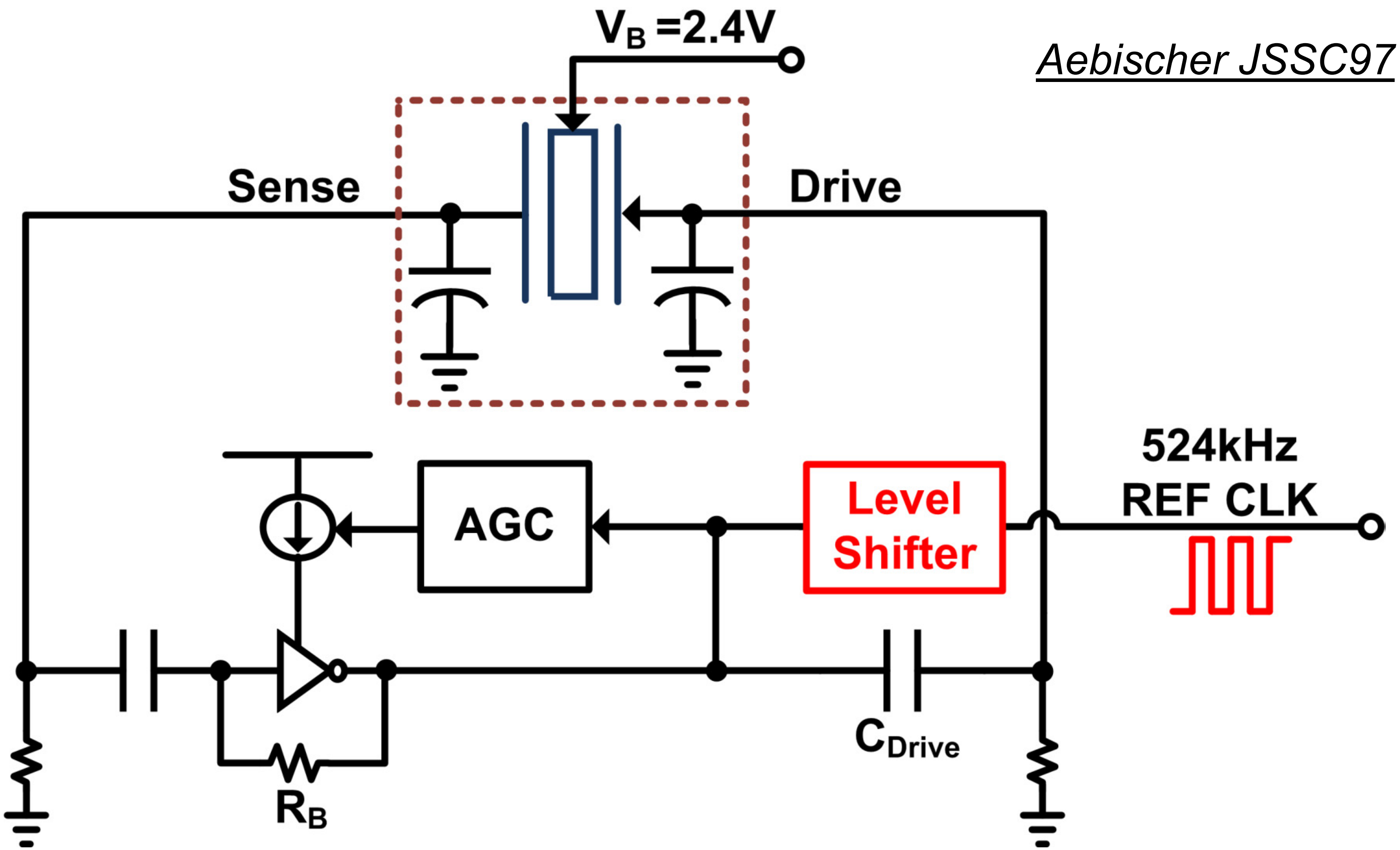
Electrical Model



R_M = 90kΩ @ V_B=2.4V

Q factor = 52,000

MEMS Sustaining Oscillator
(Pierce Configuration)



Total current consumption = 240nA

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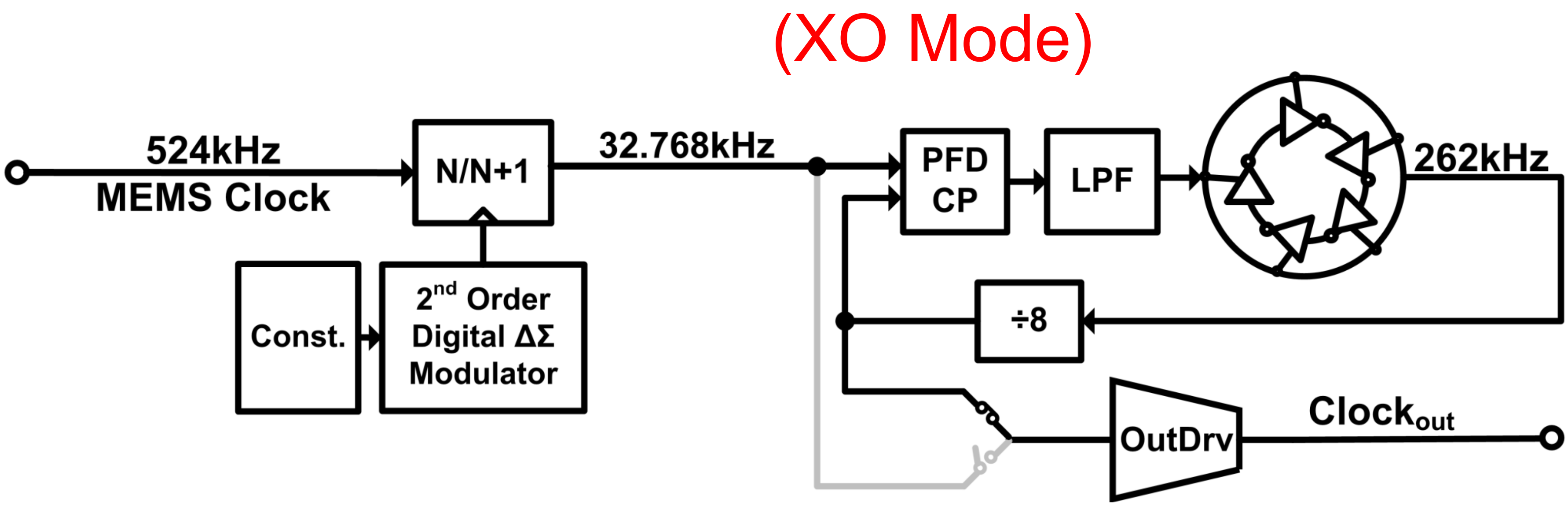
Phase Locked Loop (PLL)

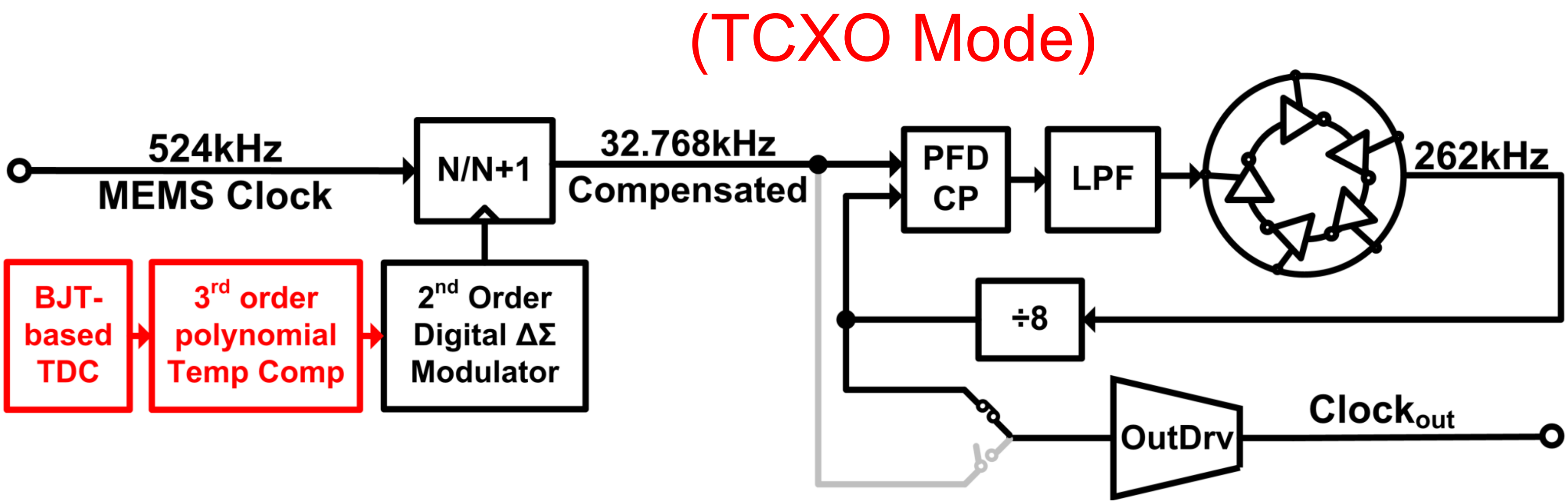


Parameter	Value
I-CP	16nA
PLL-BW	1kHz
VCO freq	262kHz
Total current	290nA

Why PLL?

✓ To filter ΔΣ modulator noise

Phase Locked Loop (PLL)



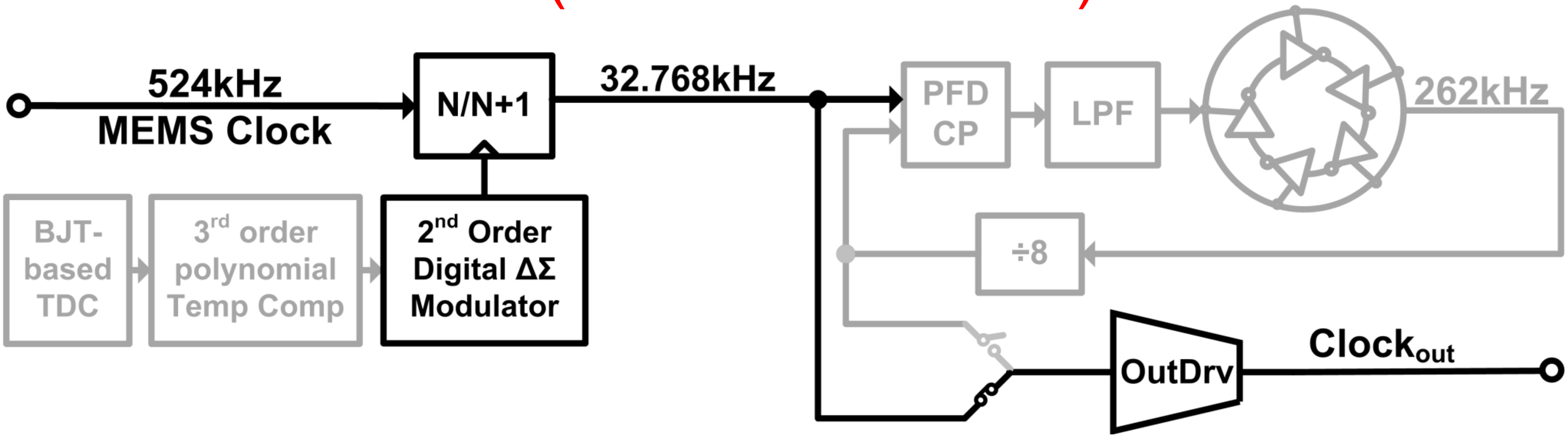
Parameter	Value
I-CP	16nA
PLL-BW	1kHz
VCO freq	262kHz
Total current	290nA

Why PLL?

✓ To filter ΔΣ modulator noise

Phase Locked Loop (PLL)

(Low Power Mode)



Low Power Mode:
- ✓ Disabled PLL
- ✓ Disabled temp compensation

Why PLL?
- ✓ To filter ΔΣ modulator noise

Parameter	Value
I-CP	16nA
PLL-BW	1kHz
VCO freq	262kHz
Total current	290nA

Outline

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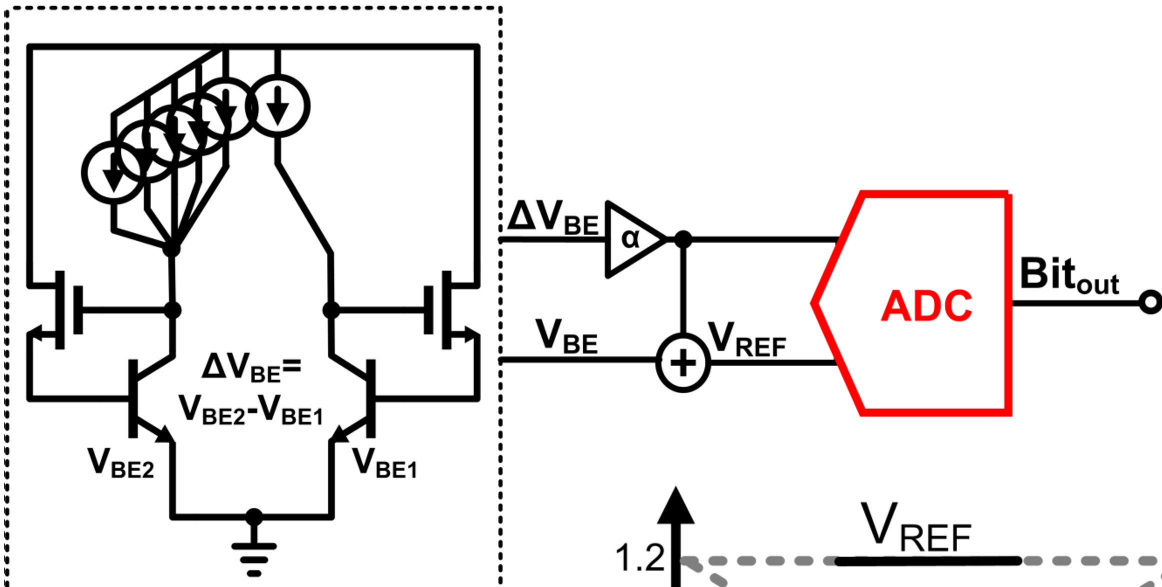
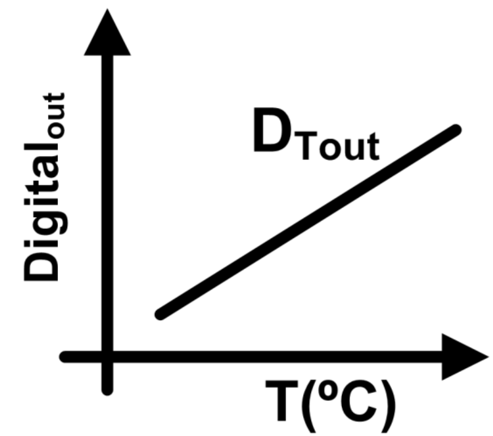
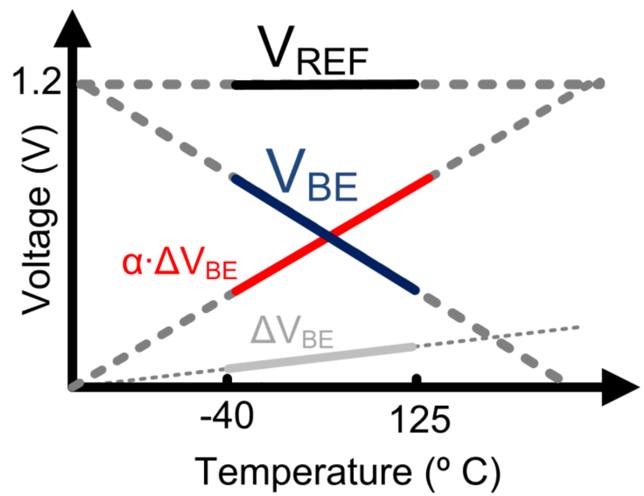
BJT-based Temperature Sensor



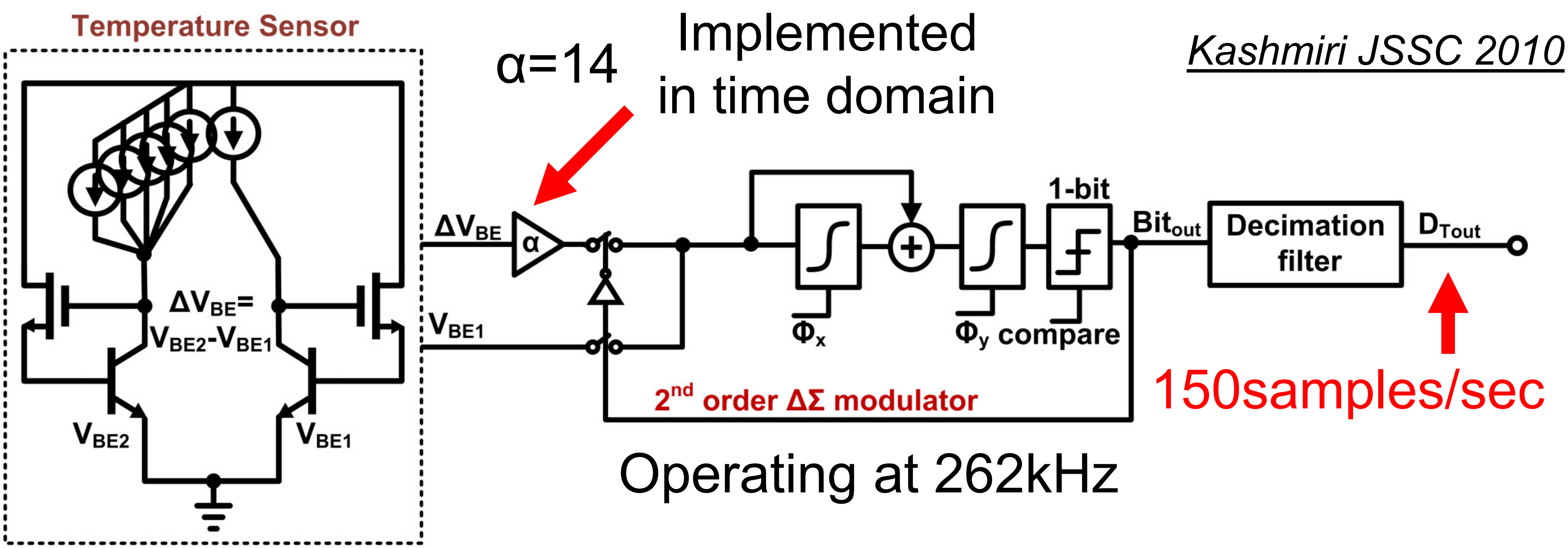
Pertijs JSSC 2005



Current	Value
BJT core	1.5µA



Temperature to Digital Converter

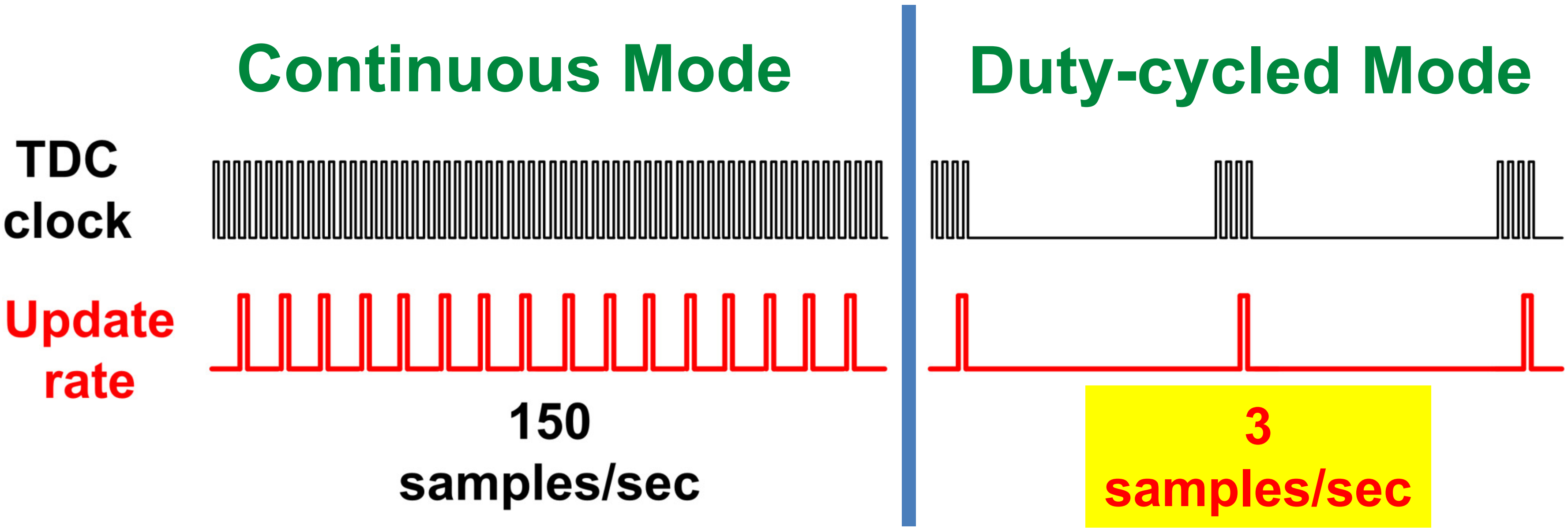


To reduce error sources:

- ✓Dynamic element matching
- ✓Correlated double sampling
- ✓System level chopping

Current	Value
1^{st} op-amp	1.2µA
2^{nd} op-amp	0.5µA
Total	4.5µA

Duty Cycling TDC
(Feature to save power)



Duty cycled TDC:

- ✓ Power down TDC in sleep mode
- ✓ Clock gating in sleep mode
- ✗ Trade off between power and temperature tracking

Current	Value
TDC	100nA

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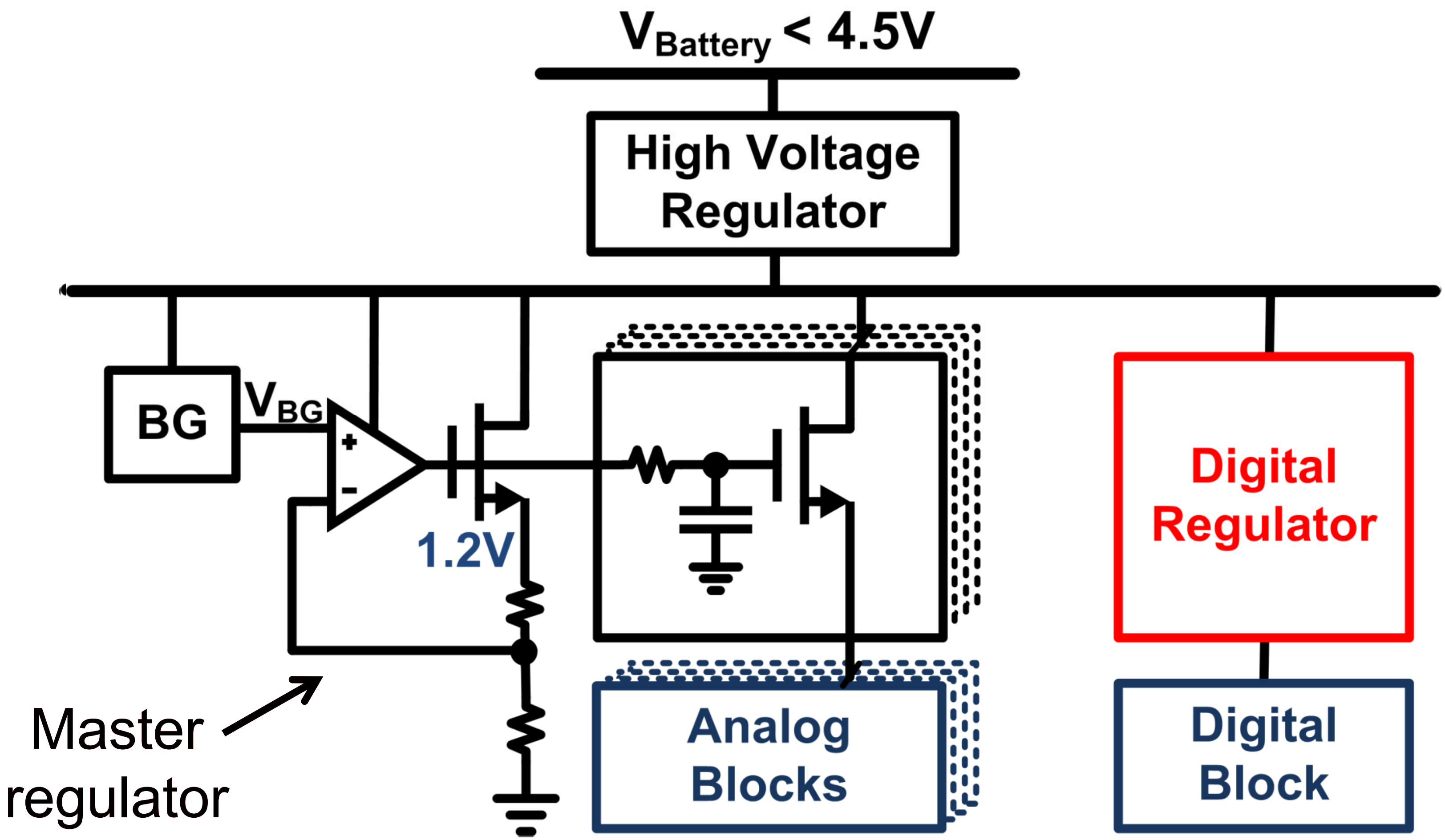
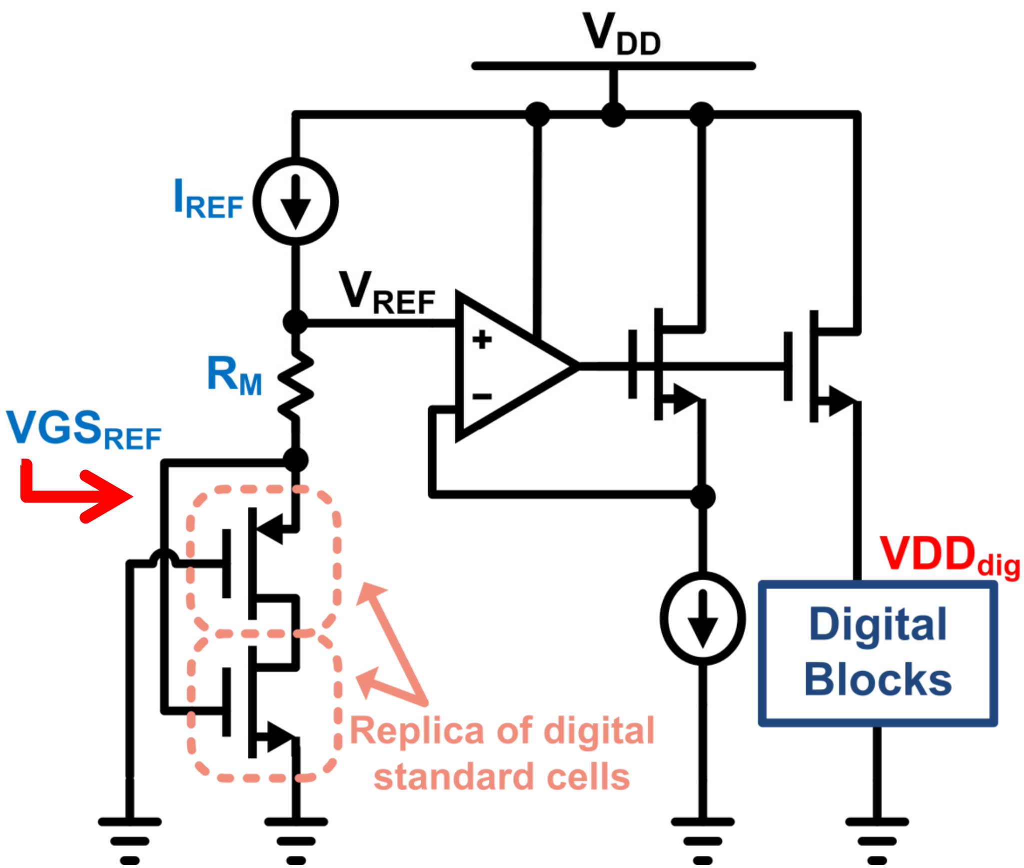
Voltage Regulator Architecture

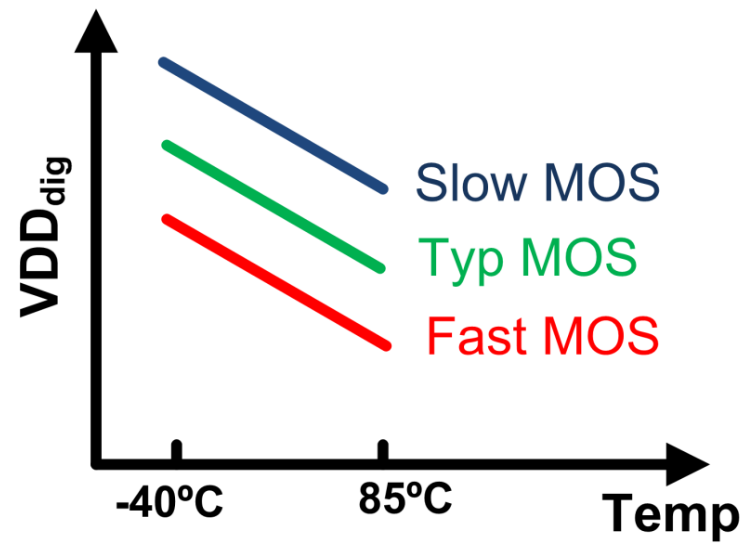


Open loop technique to save power and area

Digital Regulator

Digital supply tracks process & temperature





$$V_{REF} = VGS_{REF} + R_M \times I_{REF}$$

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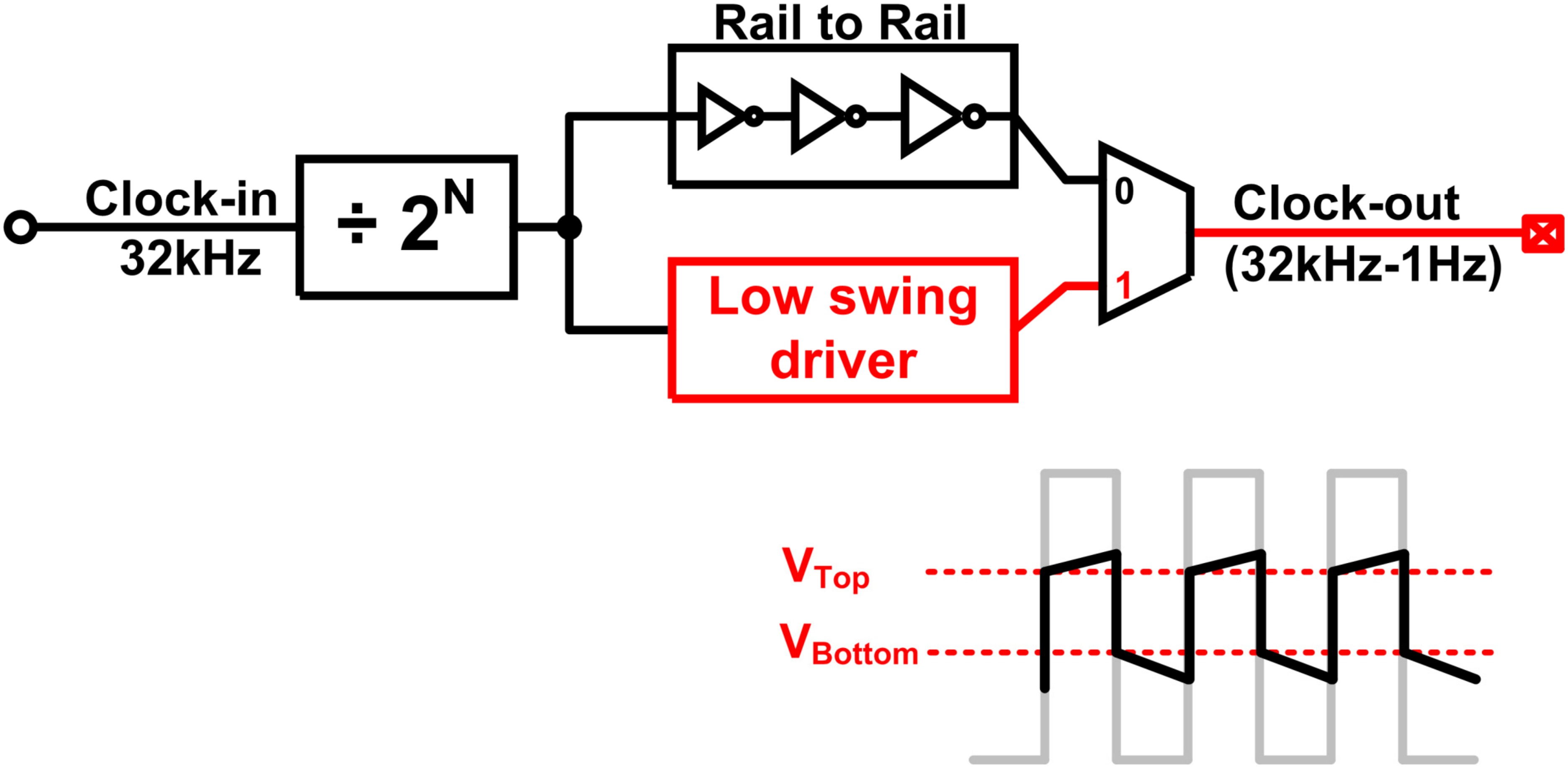
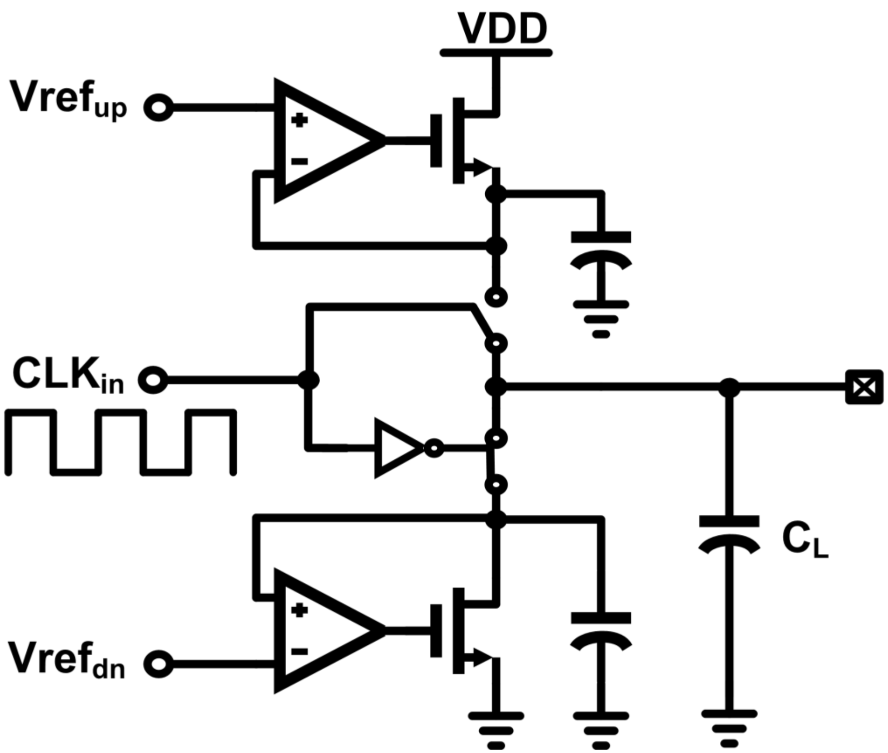
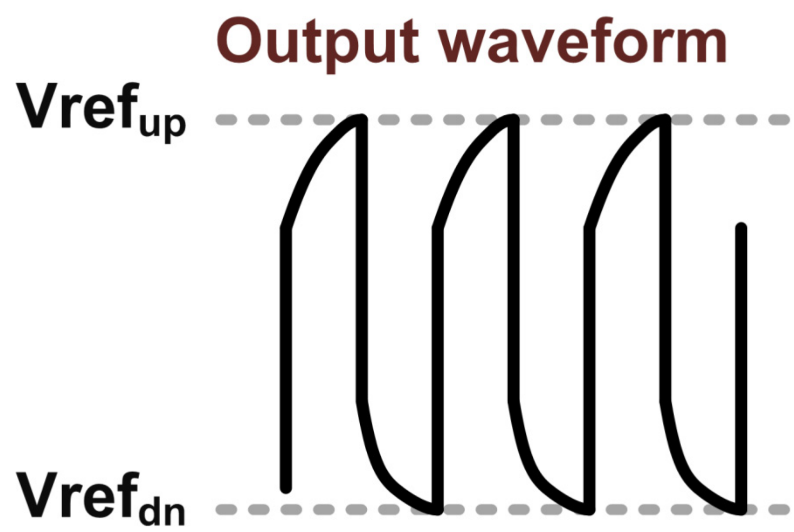
Output Driver



Goal is to limit output clock swing

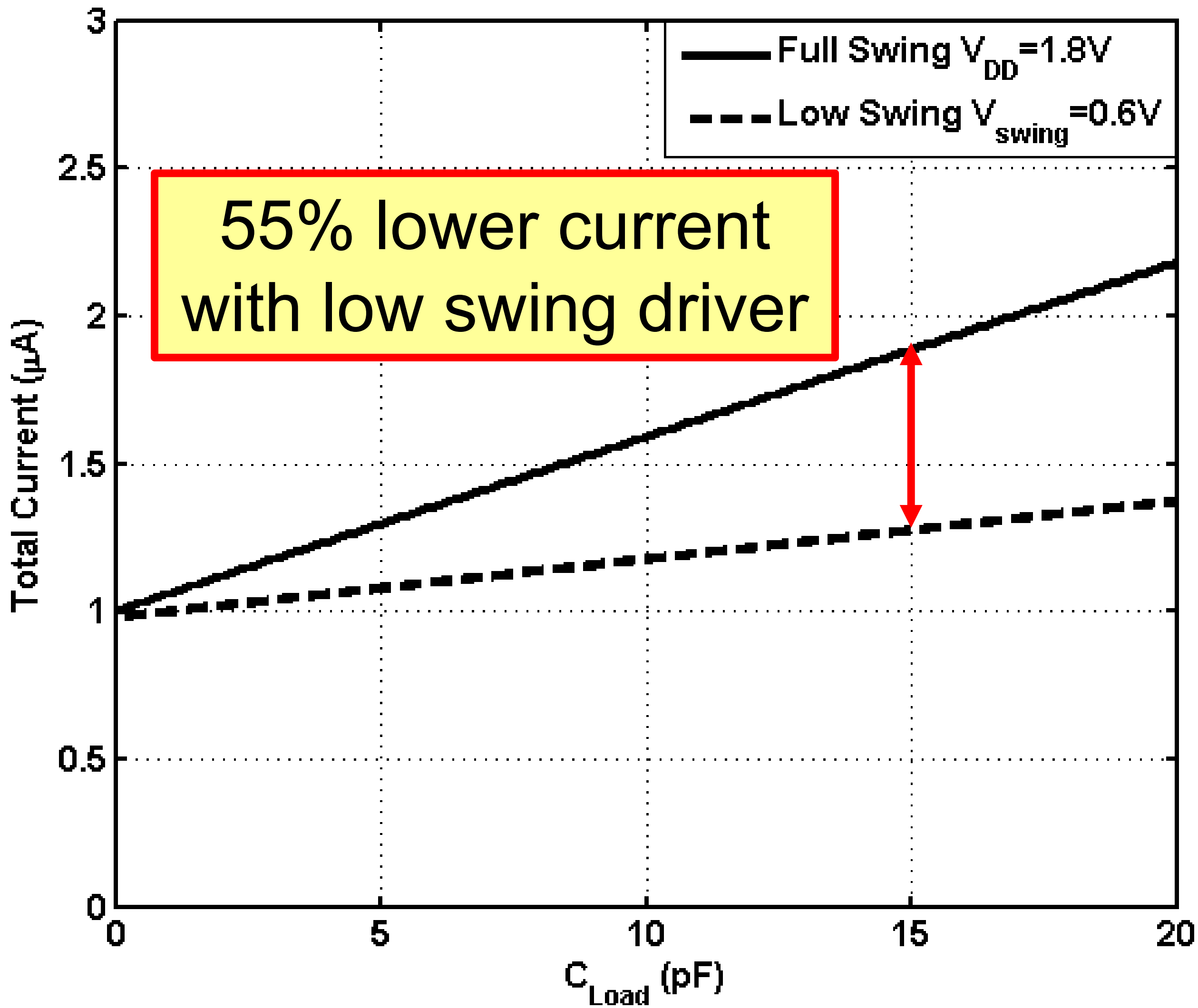
Low Swing Output Driver





Low swing to save CVF current

Comparison: Low vs. Full Swing Drivers



Outline

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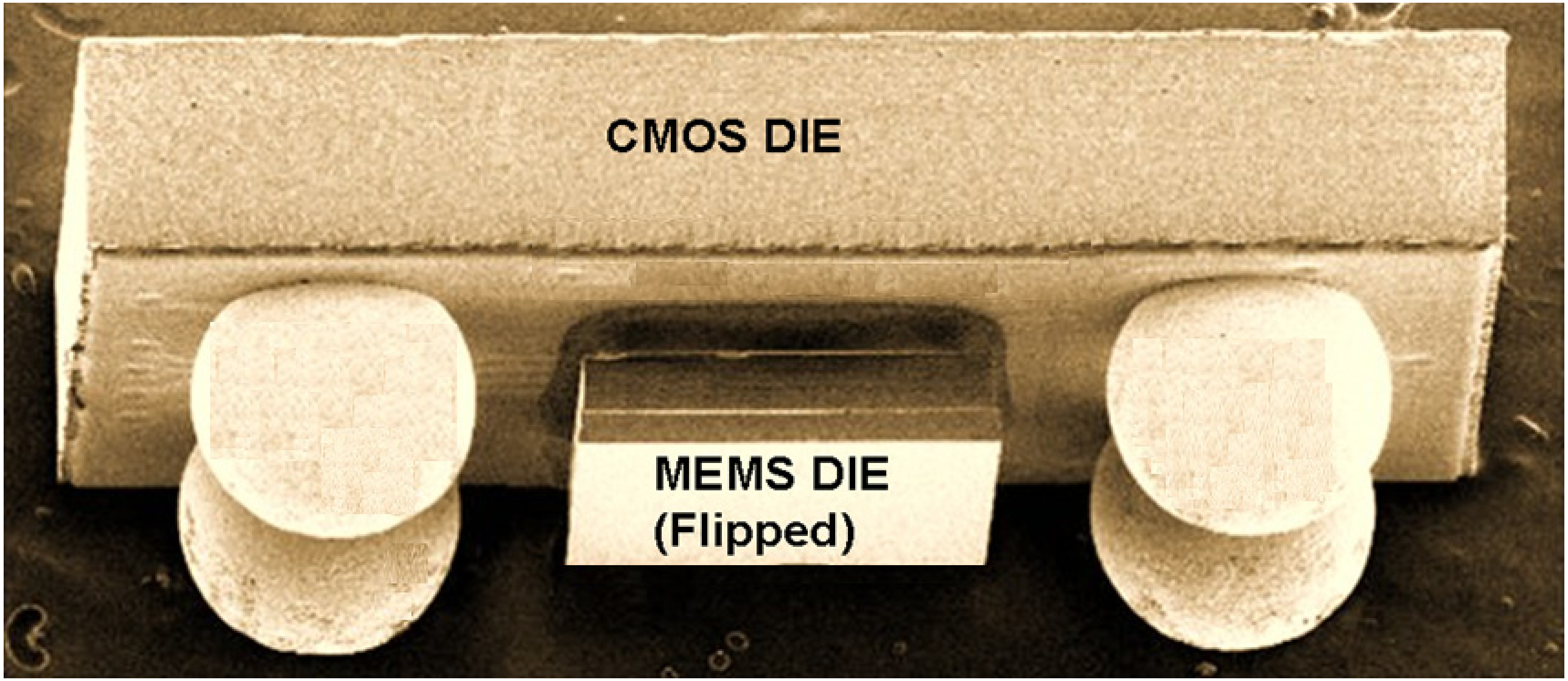
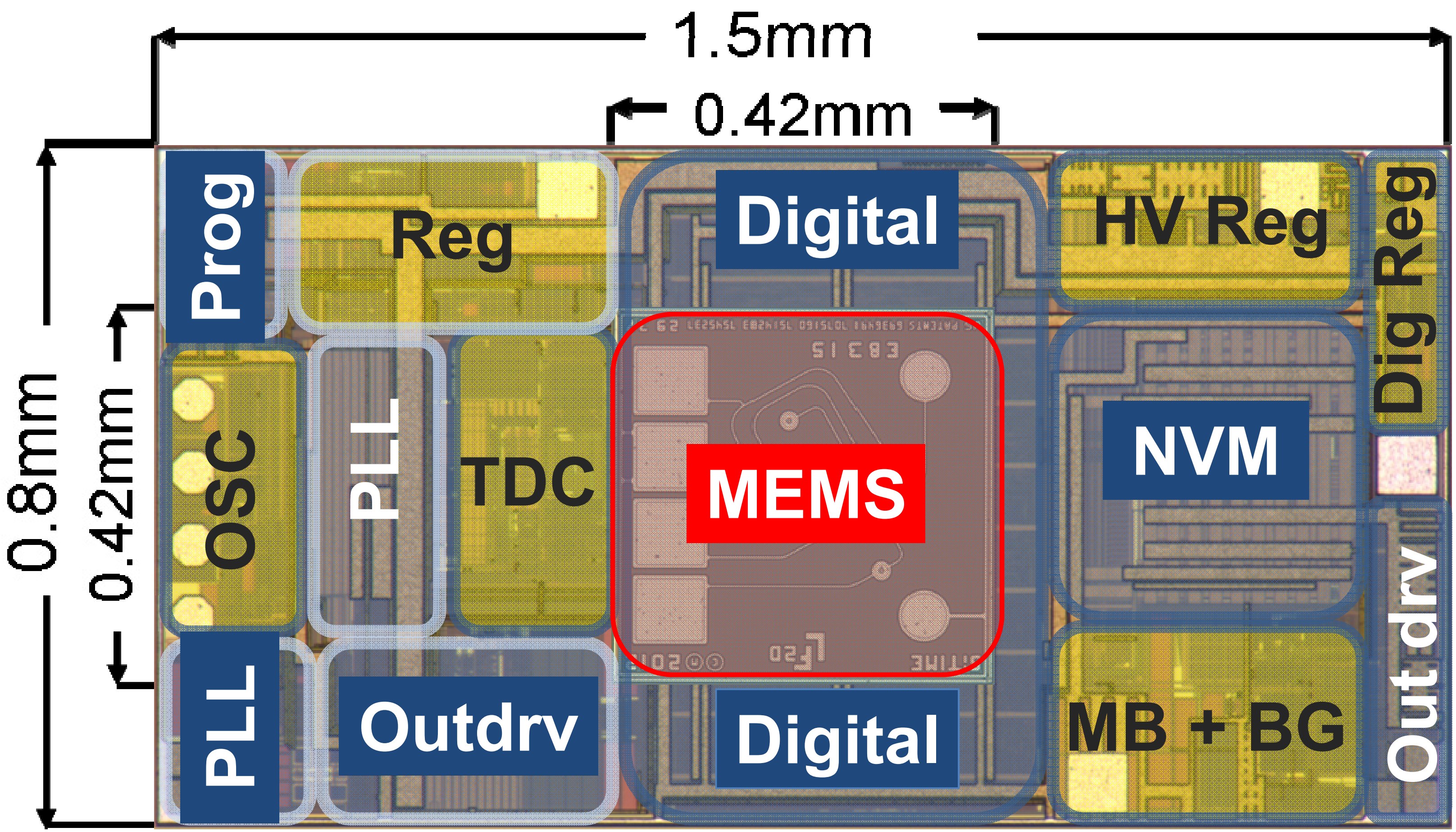
Chip Scale Package (CSP)

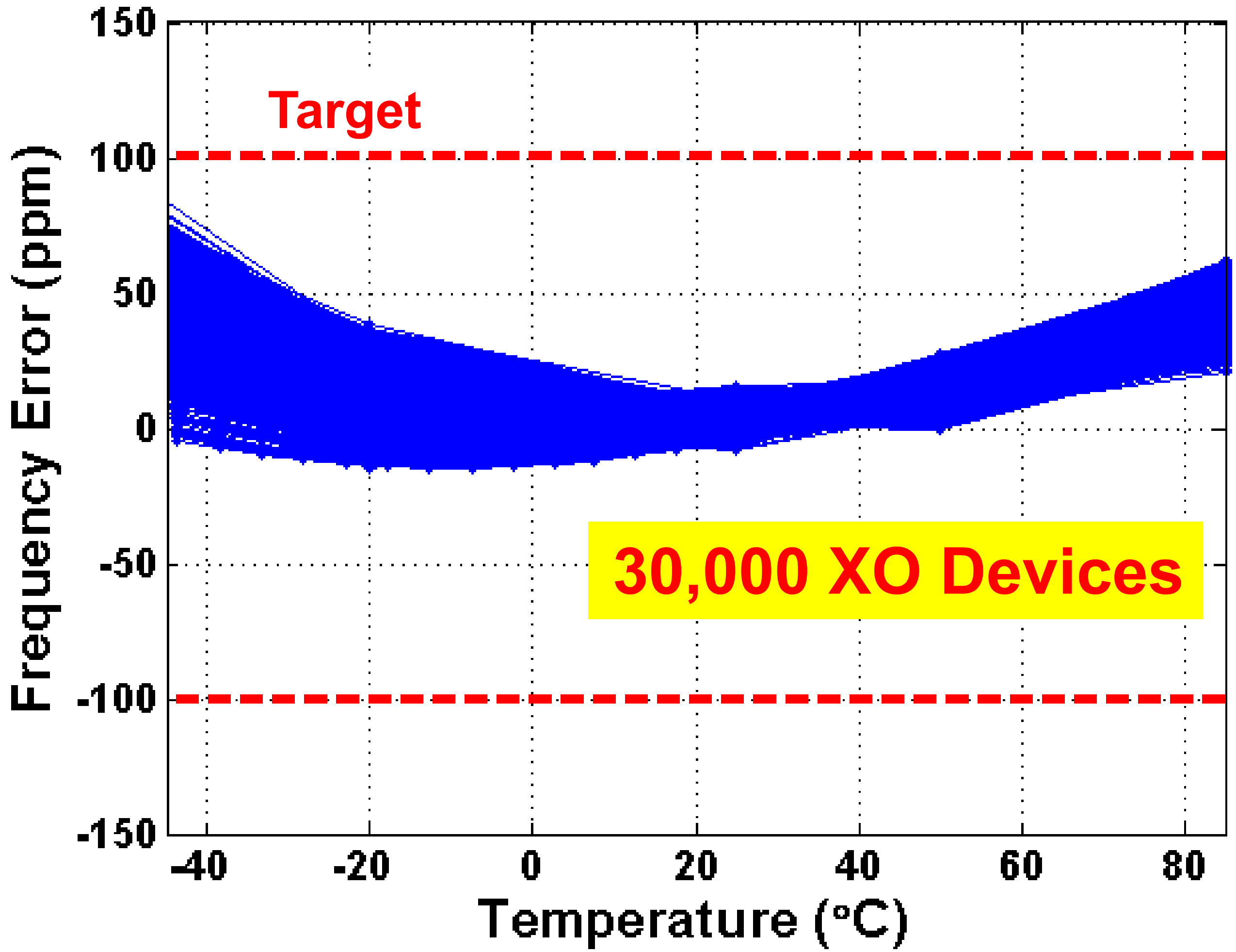
Size: 1.55mmx0.85mm



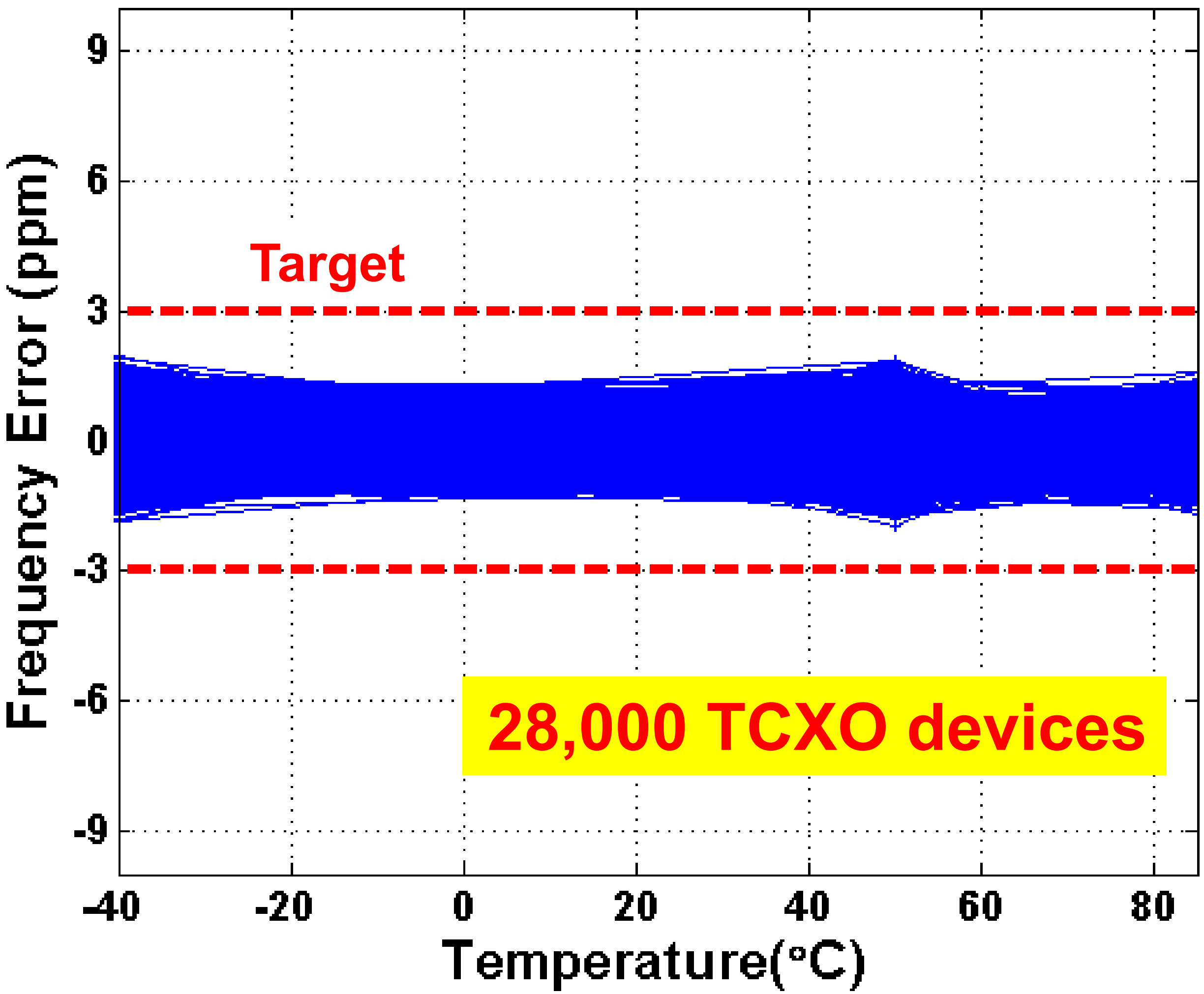
Chip Micrograph of MEMS and CMOS



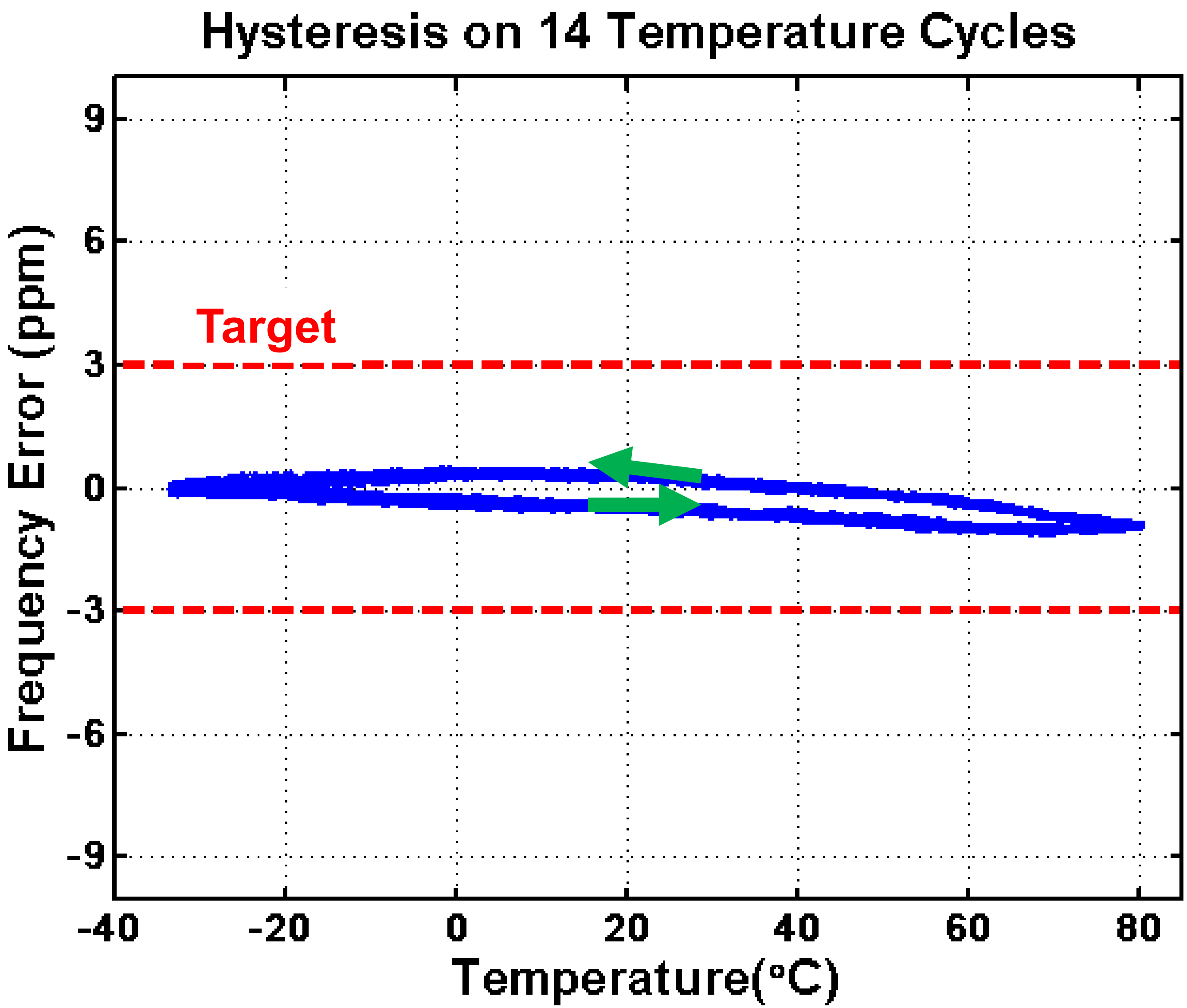
XO Frequency Error over Temperature
(Temperature compensation disabled)



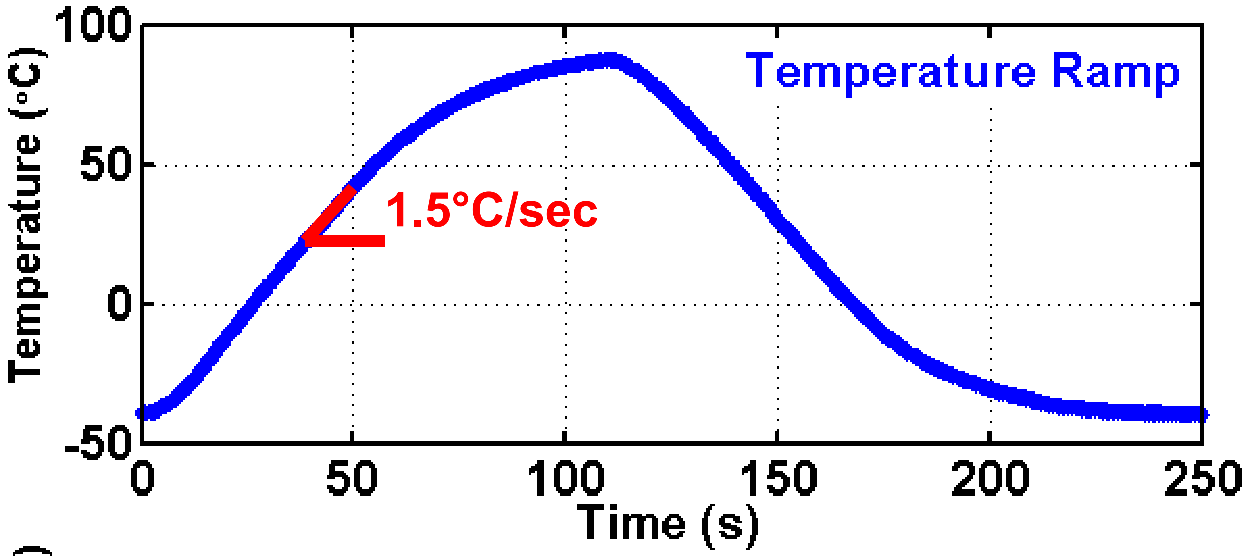
TCXO Frequency Error over Temperature
(Temperature compensation enabled)

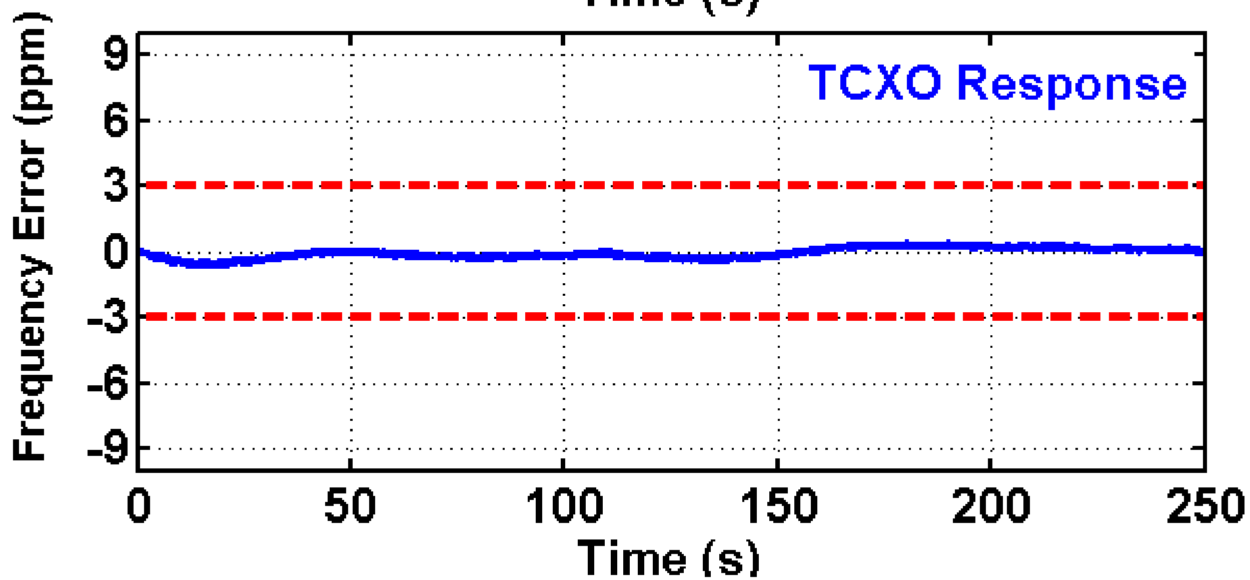


Hysteresis over Temperature

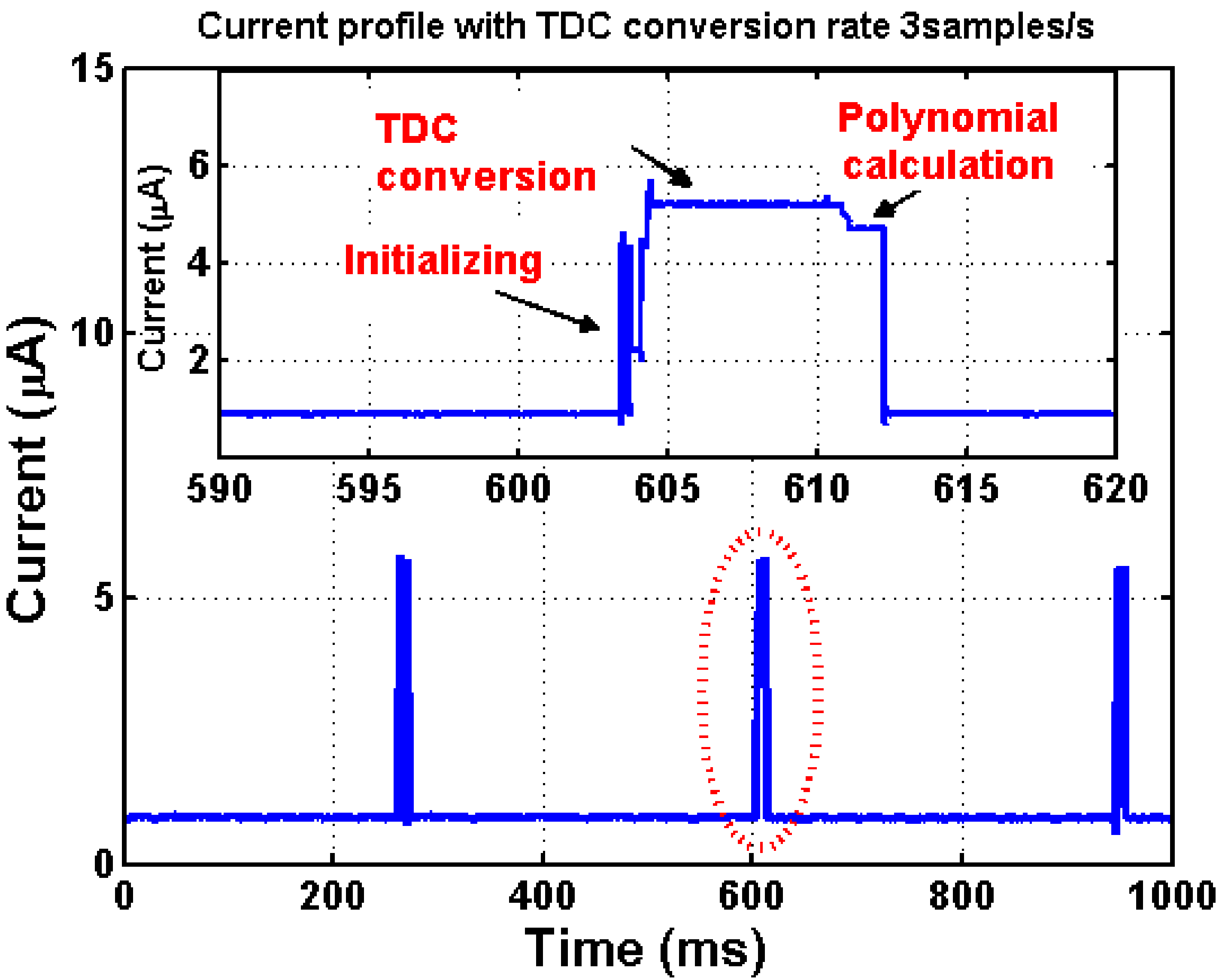


TCXO Response to Temperature Ramp





Transient Current



Comparison Table (XO)

Parameter	This work	Epson SG-3050	Micro crystal OV-7604
Supply Voltage (V)	1.2 to 4.5	1.2 to 5.5	1.2 to 5.5
Temperature Range (°C)	-40 to 85	-20 to 70	-40 to 85
Frequency Stability vs. Temp (ppm)	100 max	120 max	160 max
Supply Sensitivity (ppm/V)	± 0.25	± 3	± 1.5
Start up time (s)	0.2	1	0.5
Current (μA) (Clock enabled, no load)	0.9 typ 1.4 max 0.6 LPM	- typ 2 max	0.4 typ 0.5 max
Package Size (mmxmm)	1.55x0.85	2.2x1.4	3.2x1.5

Comparison Table (TCXO)

Parameter	This work	Maxim DS32kHz	Epson TG-3530
Supply Voltage (V)	1.5 to 4.5	2.7 to 3.5	2.2 to 5.5
Temperature Range (°C)	-40 to 85	-40 to 85	-20 to 70
Frequency Stability vs. Temp (ppm)	± 3	± 7.5	± 5
Supply Sensitivity (ppm/V)	± 0.25	2.5	± 1
Start up time (s)	0.2	1	3
Current (μA) Clock enabled, no load	1 typ 1.5 max	1.85 typ 4 max	1.7 typ 4 max
Package Size (mmxmm)	1.55x0.85	18.5x6.35	5x10.1

Conclusion

- **The smallest and lowest power 32kHz TCXO**
  - 6X smaller (1.55mmx0.85mm)
  - 2X less power (< 1.5μA)
  - Improved accuracy (3ppm)
- **Techniques to achieve this:**
  - Combining MEMS and CMOS technology
  - Sub-threshold design
  - Duty-cycling TDC
  - Open Loop regulators
  - Digital regulator to track process and temp
  - Low swing driver